

THE ELECTRONIC WARFARE APPLICATION OF  
SPECIAL PURPOSE MICROPROGRAMMED MINICOMPUTERS

Paul David Frazer

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# NAVAL POSTGRADUATE SCHOOL

## Monterey, California



# THESIS

THE ELECTRONIC WARFARE APPLICATION  
OF  
SPECIAL PURPOSE MICROPROGRAMMED MINICOMPUTERS

by

Paul David Frazer

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The Electronic Warfare Application  
of  
Special Purpose Microprogrammed Minicomputers

by

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Submitted in partial fulfillment of the  
requirements for the degree of

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from the

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June 1974



## ABSTRACT

An algorithm for the application of a special purpose minicomputer to the automatic analysis and initial classification of EW signals is developed. The minicomputer assembly language version of this algorithm is presented. A FORTRAN program which generates realistic data for signal analysis is described. Using the simulated data and an instruction level simulation program, the algorithm is tested using an IBM 360 computer. Microprogramming techniques are presented which optimize the minicomputer application.



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## I. STATEMENT OF THE PROBLEM

Electronic Support Measures (ESM) are designed to extract information about hostile forces from the electromagnetic environment they create. Since the earliest days of radar, there has been a parallel development of equipment, techniques and tactics designed to counter the use of radar by hostile forces by using the transmitted energy to detect, locate and track the hostile force, often without your own unit being detected by the searching radar system.

The current proliferation of radar systems, telemetry systems, communications systems and navigation systems which all use electromagnetic radiation for operation has created a condition of overcrowding of the electromagnetic spectrum. More important from the ESM standpoint is that the detection of a signal at almost any reasonable frequency is assured. What is not assured is being able to detect signals which are determined to be of interest in a sufficiently timely manner to be of use to the Operational Commander.

The dense signal environment which exists in world areas of interest, coupled with the rapidly decreasing allowable reaction times imposed by new and developing weapons systems, and the continuous requirement to maintain viable capabilities with a shrinking manpower force has imposed a requirement for faster, more accurate, automatic classification of ESM signals. The development of techniques for



their employment in the task of signal analysis in the ESM environment.

To date, the major effort has been to apply digital computers to the task of off-line signal analysis and specific threat identification problems. What is now required is the expansion of these or similar techniques to handle the task of routine surveillance over a wide frequency range, filtering received information for interest, determination of the parameters of received signals, initial classification and threat evaluation, and display to an operator or output to a remote location. All of this has to occur in real time with a high probability of developing correct information. It is felt that such a system may be feasible if it is designed taking advantage of the rapid data handling capability of digital computer systems specifically designed for this application.



## II. CONCEPTUAL SYSTEM DESIGN

### A. SYSTEM OPERATIONAL REQUIREMENTS

A system designed to fulfill the needs of automatic ESM surveillance classification and threat analysis has the following characteristics for effective performance.

- a. Broad frequency range.
- b. Simultaneous reception of all frequencies within the frequency range.
- c. Means of determining received signal characteristics within a reasonable accuracy.
- d. Ability to operate successfully in dense environments with tens or hundreds of thousands of pulses per second being received.
- e. Ability to associate received pulses and other forms of radiation into pulse trains or other forms for identification and analysis.
- f. Means of determining the bearing of the received energy to within acceptable accuracy.
- g. Accurate means of identifying signals as to class and probable source.
- h. High probability of intercept.
- i. Low false alarm rate.

### B. SYSTEM COMPONENTS

Conceptually such a system could be assembled using a series of Instantaneous Frequency Measurement (IFM) receivers



that would cover the frequency bands of interest. The outputs of these receivers would be applied to small special purpose digital computers which would perform the initial information filtering task of creating a data set of the parameters of all of the received pulse trains and exclude from further processing those signals which are obviously of no interest to the tactical environment. Information thus derived is then to be passed to a second computer system at considerably lower data rates which will allow detailed analysis of signals, final classification tasks and automatic threat evaluation.

Detailed design of an entire system such as that described is beyond the scope of this thesis. The problem area specifically treated is the first interface between the IFM and the associated digital computer and the information filtering task it is required to do.

### C. SPECIFIC SUBSYSTEM DESIGN ANALYSIS

The specific design problem analyzed herein is stated as follows.

Given an IFM receiver with an omnidirectional antenna and reasonable sensitivity and probability of detection at all frequencies within its band width, analyze the feasibility of providing a special purpose digital computer that will accept all information developed by the IFM and provide as real-time outputs the frequency, pulse width, pulse repetition interval, scan type and the time of last intercept.





### III. COMPUTER SELECTION FOR PURPOSES OF FEASIBILITY ANALYSIS

To complete the analysis of the feasibility of the automatic IFM system, it was desirable to actually encode and simulate the operation of the system using an existing computer instruction set. It was also of interest to determine the required execution times, pinpoint improvements to the basic algorithm, establish required additional 'special case' instructions which could improve the efficiency of execution, and establish desirable hardware arrangements which would enhance the overall operation of the computer. Through the experience of operating a simulation program and the test of various software and hardware techniques, the detailed specifications for a special purpose computer can be determined. This computer would be specifically designed and optimized for the demanding high data rates anticipated. Investigation disclosed the existence of a small high speed special purpose computer produced by Applied Technology Corporation (ATI) in Sunnyvale, California. This computer is designated as the Applied Technology Airborne Computer (ATAC) and is a 16 bit fixed point 2's complement machine. A number of unique features of this computer made it an obvious choice for this study. The general computer characteristics and these special features are summarized below. Further detailed information is available in ATAC, Applied Technology Airborne Computer, Vol. I, Principles of Operation.



1. 16-bit instruction word length with a 437 nanosecond major cycle time.

2. Sixteen general registers.

3. Four basic instruction addressing modes with three supplemental modes allowing a wide range of direct, indexed and immediate execution instructions.

4. Asynchronous memory with provisions of up to 4 Direct Memory Access channels.

5. Memory types can be mixed in any combination of Read Only Memories (ROM), Bipolar Random Access Memories (RAM), Read Mostly Memories (RMM) and slower core memory devices.

6. Twelve main priority interrupts.

7. 16-bit parallel input/output operations.

8. Extremely small size and power requirements: 6 pounds, 115 cubic inches, and a power consumption of approximately 70 watts for a nominal configuration.

9. An existing software support package designated as the ATAC Programming Support System (APSS).

10. Microprogrammed instruction set allowing ease of modification of the instruction set within the hardware limitations of the machine.

11. Computer assisted hardware design and fabrication allowing relative ease and speed of modification of the hardware configuration (within limits) to permit optimization of the computer for specific applications.

The features listed under 9, 10 and 11 are the essential features required for this feasibility study. As the basic



speed, memory configuration and programming flexibility required are provided by the existing ATAC, arrangements were made with ATI to allow use of portions of the APSS for this effort.

#### A. ATAC PROGRAMMING SUPPORT PACKAGE (APSS).

APSS is a computer simulation program designed and programmed for use on IBM 360/370 series Operating Systems.

The complete package consists of the following items.

##### Volume 1 - ATAC BASIC PRINCIPLES OF OPERATION

This document describes the basic ATAC machine characteristics and the instruction set.

##### Volume 2 - ATAC PROGRAMMING SUPPORT SYSTEM (APSS)

APSS is the support software system for ATAC which allows preparation and debugging of programs via an IBM 360/370 computer system.

The documents in this volume describe how to set up and use the APSS system and includes publications describing the PL/ATAC Compiler, Assembler, Loader Simulator and microprogramming facilities.

Section I - APSS Job Management

Section II - PL/ATAC Compiler

Section III - APSS Assembler/Loader

Section IV - APSS Instruction-Level Simulator

Section V - APSS Microprogramming Software



### Volume 3 - ATAC SYSTEM DIAGNOSTIC PROGRAMS

This document summarizes the use of ATAC's Diagnostic programs for instruction test, I/O test, interrupt system checkout, and condition code test.

### Volume 4 - ATAC CIRCUIT BOARD TEST PROGRAMS

This document summarizes the ATAC circuit board test procedures.

### Volume 5 - ATAC OPERATOR'S GUIDE

Procedures for the operation of an ATAC computer are described in this document.

### Volume 6 - ATAC 16A MICROPROGRAMMING AND SIMULATION

Procedures for developing microprograms for the ATAC 16A central processing unit.

The portions of APSS utilized for this study are listed below. Other volumes were not required but their existence is noted. Future efforts in the development of specifications for a special purpose computer should be made with the knowledge that such systems exist. The advantages accrued by having a computing system specifically tailored to the task at hand are self evident. Additional flexibility is provided through the use of microprogramming in that a completely different instruction set can be defined by replacing the microprogram Read Only Memory allowing the same basic machine to be optimized for several different tasks and reconfigured by changing a small inexpensive module.





Volume 1 - ATAC BASIC PRINCIPLES OF OPERATION

Volume 2 - ATAC PROGRAMMING SUPPORT SYSTEM (APSS)

Section I APSS Job Management

Section III APSS Assembler/Loader

Section IV APSS Instruction Level Simulator

The APSS Instruction Level Simulation Program is currently a resident program on the IBM 360/67 at the Naval Postgraduate School. Details concerning the implementation of the program are contained in Appendix A. Details concerning its use are contained in Appendix B.



#### IV. THE IFM DIGITAL PROCESSOR

The initial design concept for the interface between the IFM and the special purpose digital computer is a common memory storage area to which both units have Direct Memory Access on a non-interrupt basis. The data to be passed between the IFM and the computer consists of the frequency, pulse width and time of arrival of all received signals. Using this information, the computer can classify signals as pulsed type radar signals based on the indicated pulse width. Further analysis is conducted by establishing initial pulse files segregated by frequency and ordered by the sequence in which they were received. An estimate of the PRI is made by averaging the time between the arrival of adjacent pulses in the file. Small variations in the PRI estimate are treated as noise. Large variations in the time between pulses are considered caused by antenna scan characteristics. Variations between these extremes are considered due to the superposition of multiple pulse trains or due to a complex PRI 'jitter' imposed on the emitter. Variations due to noise and antenna scan are handled internally. Variations due to interleaved pulse trains and complex jitter patterns are signalled and further analysis of these cases is handled by the main classification computer. The design calls for the special purpose IFM computer to output the following information for each pulse train received.



- a. Frequency
- b. Pulse width within limits, the value
- c. Pulse width out of limits, a designation
- d. Stable PRI, the value
- e. Unstable PRI, a designation
- f. Antenna scan time
- g. Time of last update
- h. When ordered, a pulse train of specified length to be used for analysis of complex signals by the main classification computer.

#### A. TIME ENCODING

Determination of the pulse width and the time of arrival requires a digital clocking system whose output is directly translatable into real time. For purposes of analysis it is assumed that when the IFM threshold is exceeded in a specific frequency band, the current value of the clock is loaded into the time of arrival words. Simultaneously the pulse width word is cleared and then incremented at the clock rate. When the pulse energy ceases, the pulse width word contains the pulse width scaled by the clock rate.

The clock consists of a 40 bit counter. The clock rate is 10 Megahertz. This corresponds to a least significant bit value for pulse width of 0.1 microseconds. The pulse width word consists of bits 0-15 of the counter which allows representation of pulse widths of up to 6.5 milliseconds treating the most significant bit as a magnitude



instead of a sign bit. The time of arrival double precision word consists of bits 8-39. This corresponds to a least significant bit value of 25.6 microseconds. The maximum clock time (time to overflow) is 15.3 hours. The most significant bit of the clock is treated as a sign bit to allow detection of the data out of sequence condition.

Accuracy is determined by the stability of the basic clock oscillator. Measurement is made to within 0.05 microseconds for pulse width and to within 12.8 microseconds for PRI.

## B. THE COMMON MEMORY BLOCK

The common memory block is used as a large buffer to match the differing data rate handling capability of the IFM and the computer. For purposes of analysis, it is assumed that the IFM can respond and prepare a series of four data words in the times achievable using TTL logic circuitry. This allows the IFM to load the double precision words for time of arrival and the word for frequency first, the word for pulse width as soon as the pulse has completely been received and accomplish the entire transfer of the four words in approximately 3 microseconds or the pulse width of the received signal + 0.5 microseconds whichever is longer. For signals with pulse widths of less than 3 microseconds, the IFM data will have a maximum burst rate of approximately 300 KHZ.

Simulations conducted using the algorithm described in Chapter IV indicate the average time required for the computer





to process each received pulse including read and write times is approximately 45 microseconds with improvement to 35-40 microseconds considered readily possible. This corresponds to a maximum average data rate of approximately 22,000 pulses per second.

The IFM loads data words into the common memory block sequentially starting from the '0' location and wraps around when the block is full. Also starting from the '0' location, the computer accesses the data words and associates them with the appropriate pulse train and then accesses the next word. The size of the buffer establishes the length of the time that transitory high data rates can be sustained by the system before the computer is 'lapped' by the IFM input. In this case, the computer is always accessing the most recent data set and the information stored by the IFM previously is lost. When the data rate decreases, it may become possible for the computer to catch up to the IFM to remove the lap condition. In this case, the data read by the computer will be out of sequence and will be discarded.

Pulse information is stored in the common memory block in a series of four words per pulse. These words are defined as follows.

a. Frequency. Frequency is represented by an integer corresponding to the frequency bin in which the detection occurs.

b. Pulse width. The pulse width is represented by an integer which is a scaled time value.



c. Time of arrival. Time of arrival is expressed as a double precision integer, the lower half of which is the third word, the upper half the fourth word.

The computer can keep track of the existence of new data in the word block associated with an individual pulse by resetting the frequency word to 0 after it is read. By testing the frequency word, the computer establishes whether the IFM has loaded new data since its last look at this location.

By making the IFM output and the computer input completely independent and asynchronous in operation, timing and interrupt communications, with their high time overhead costs are avoided.

#### C. THE IFM COMPUTER ALGORITHM

An algorithm has been developed which defines the operations required to develop pulse trains and extract PRI information from the IFM output data. This algorithm causes the computer to read a memory location and determine if data is available. If the data is available, the frequency word is used as a relative address to enter a file which provides linking information for the pulse train files developed for that frequency. This file data word is utilized as two half words. The lower half is used as a pulse train file pointer. The upper half is used as a pointer for an overflow storage area in the event there are two or more pulse trains associated with a given frequency.



The primary means of pulse train association is by frequency discrimination.

The pulse train file pointer is used as a relative address for entry into a contact file entry table. The table entry corresponding to the pulse train file pointer contains two words. The first word contains the frequency of the pulse train for cross reference purposes. The second word contains the absolute entry address of the actual file.

The pulse train file is used both to accumulate data for calculation of parameters and to provide output information to the main classification computer by using Direct Memory Access techniques. The file is a block of 64 memory locations which are treated as 16 four word groups. This allows storing information on 16 consecutive pulses which are used to develop an estimate of the PRI. Before 16 pulses have been received, the file is said to be building. After 16 pulses have been received and the PRI estimated, the file is said to be closed. If no current pulse information is contained in the file, it is said to be empty. The distinction is required because the contents of the words of the file have different meanings for the different cases. The contents of the file words are described below. The choice of 16 pulses used for PRI determination is arbitrary and additional testing and evaluation is required to determine the optimum number of pulses considering detection probabilities, normal antenna scan rates, false alarm rates, and simulation and operational experiences.



1. File building.

a. Word 1. Pulse width of the initial pulse detected when the pulse train file was established.

b. Word 2. Counter indicating the number of pulses stored in this file. The counter counts from -16 to 0.

c. Word 3, 4. Double precision time of arrival of the first pulse.

d. Word 5. Pulse width of the second pulse.

e. Word 6. Time difference between the arrival of the second pulse and the first.

f. Word 7, 8. Double precision time of arrival of the second pulse.

g. Succeeding groups of 4 words are arranged in a similar fashion with the second word of the group containing the time interval between the pulse and the one preceding it.

2. File closed.

a. Word 1. Average pulse width of the file.

b. Word 2. A positive integer represents the average PRI. If the location contains a zero, a stable PRI cannot be determined.

c. Word 3, 4. Double precision time of last information update.





d. Word 5, 6. Double precision time of arrival of the first pulse of the latest consecutive group of pulses to be received.

e. Word 6, 7. Double precision antenna scan rate.

### 3. File empty.

The file empty condition is indicated by the first word of the contact file entry file being zero. The contents of the pulse train file should be considered as being unspecified.

The scheme of using the frequency as a relative entry address to the frequency file, using the data contained in the frequency file as an entry into a contact file and using the data contained in the contact file to provide the actual address of the pulse train file is required to maintain pulse train files without the requirement to have a separate pulse train file for every possible combination of frequency and pulse width. A total of 64 pulse train files can be established and maintained simultaneously in the current configuration.

In the event that two pulse trains of differing pulse widths are received in the same frequency bin, provision has been made to discriminate these signals by pulse width and establish and maintain separate files on these signals. If interleaved pulse trains of nearly equal pulse widths are received on the same frequency, the algorithm will consider the pulse train as having a complex PRI and enter a zero in the PRI word. The main classification computer can



then designate the requirement to establish a file of sufficient length to collect enough pulses for analysis by inserting the required number of pulses into the PRI word. After filling 60 of the 64 assigned locations for the pulse train file, the remainder of the long file is inserted into an overflow section of memory. Words 61-64 are used to provide linking information.

Calculation of the PRI after 16 pulses have been received is accomplished by averaging the time interval between pulses. Sixteen pulses are contained in the pulse file and the seventeenth pulse to arrive causes the start of this calculation to provide 16 time intervals for the averaging. The intervals are treated in reverse order of their appearance. The latest interval is treated as a standard and the previous interval is compared with it. If the two intervals are not nearly equal, the condition of one being nearly equal to a multiple of the other is checked for multiples up to 4. If this condition is met, both intervals are made equal to the smaller interval and their sum is accumulated. If the condition is not met, both intervals are still made equal to the smaller interval (the longer interval discarded) their sum accumulated and a discard counter is incremented. The process is repeated with the other time of arrival increments in the file until all 16 intervals have been summed or until the discard counter reaches 4. If 4 pulses are discarded, the PRI is considered unstable and a zero is inserted into the PRI word. If all 16 pulse intervals are



summed, the resulting sum is divided by 16 (shifted right 4 bits) and the result inserted into the PRI word. Concurrently, the pulse widths are also summed to calculate the average pulse width of the file in a similar manner.

After the file has been closed, succeeding pulses received are utilized to update the data in the file. If a received pulse width is within limits of the file pulse width, it is compared with the file pulse width to determine its relative size. If the new one is smaller, a 1 is subtracted from the file pulse width. If larger, a 1 is added. This feature ensures that long term drifts in the parameter value can be tracked. If a PRI has been established for the file, and the time interval between succeeding pulses exceeds established limits, the new pulse is considered to have established simple antenna scan parameters and an antenna scan rate estimate is calculated.

The IFM computer algorithm is shown in flow chart form in Figure 1.



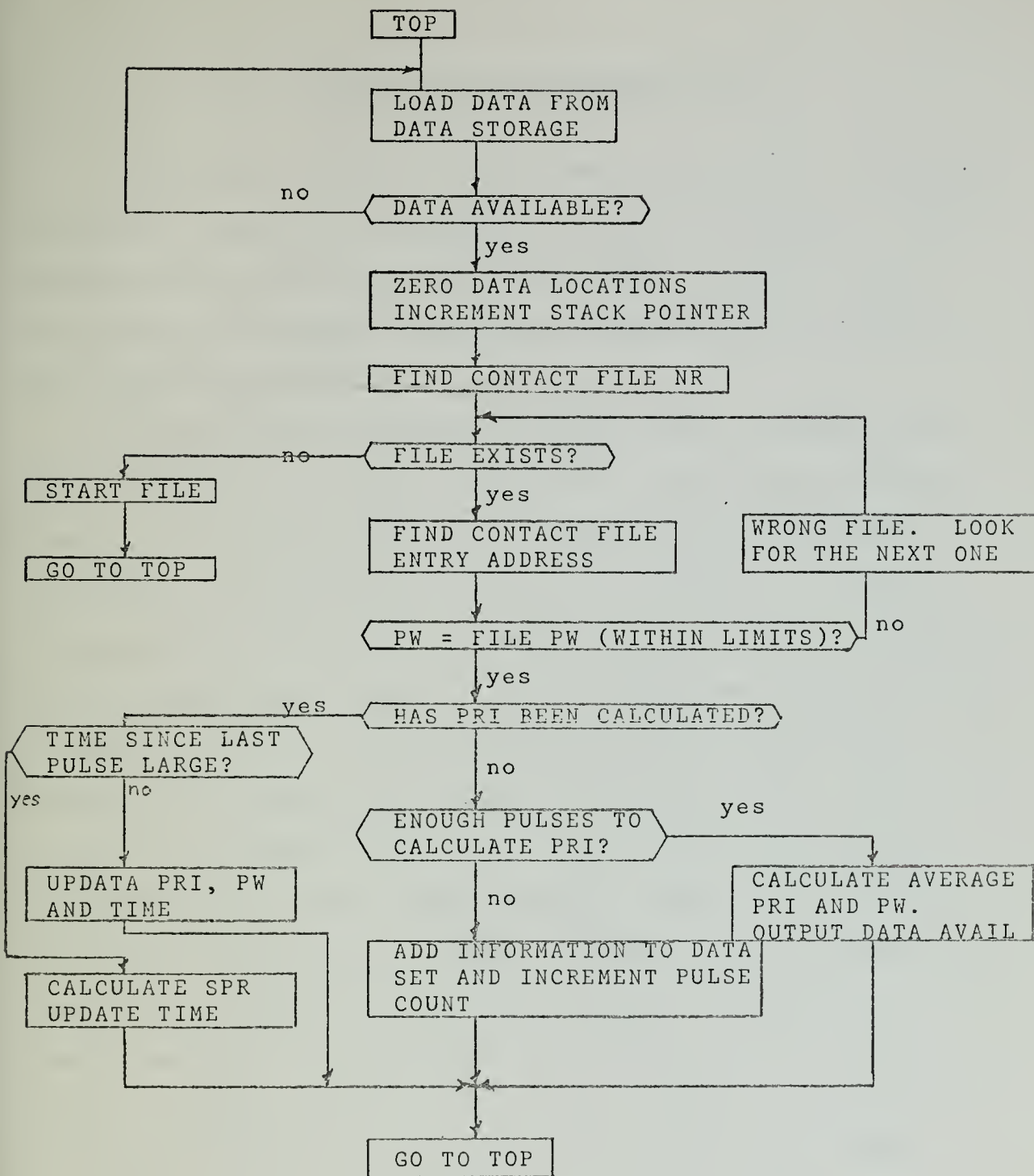


Figure 1. THE IFM DIGITAL PROCESSOR ALGORITHM  
(SIMPLIFIED FLOW CHART)





## V. DATA SIMULATION PROGRAM (DSP)

The DSP was written by the author to provide a relatively realistic input data environment to the ATAC Simulator. The program was written well before the ATAC Simulator became available and includes many features which are not useful in its current application.

The DSP provides simulated signal levels arriving at an IFM receiver in a dynamic environment. Input data provides initial set up positions for the IFM and up to 10 emitter platforms. The IFM and all of the 10 platforms are given courses and speeds which are used to update their positions as the simulation proceeds. Each platform may have up to 5 emitters on board of any specified frequency, PRI, PW, anetnna scan, antenna gain, and antenna beam width. The program establishes the initial antenna position by using a uniformly distributed random variable, updates the antenna position, calculates the signal strength of each transmitted pulse when received by the IFM and outputs those pulses which are above the specified threshold sensitivity of the IFM. The output consists of the time sequence of pulses received by the IFM including the frequency, pulse width, time of arrival, bearing and signal strength.

The data used by the ATAC Simulator consists of four integers for each pulse. These words are:

1. Frequency bin. The bins are numbered in ascending order of frequency from 1-128 although the only restriction



is that there has to be less than a total of 255 bins for the current ATAC Simulator program and the 0 bin cannot be used as it is used by ATAC to signal a no data state.

2. Pulse width. The pulse width word is an integer in the range 0-65,535. Any time scaling factor may be used. The current convention adopted is that the integer 1 corresponds to a time interval of 0.1 microseconds. This allows representation of any pulse width from 0-6.5 milliseconds to within 0.05 microseconds.

3. Time of arrival. Time of arrival is expressed as a double precision (32 bit) integer. Word 3 is the least significant half of this integer and holds time values up to 0.84 seconds with the least significant bit corresponding to 25.6 microseconds.

4. Time of arrival. The upper half of the time word holds time values up to 15.3 hours. This clock update rate and time measurement accuracy is considered adequate for contact analysis and PRI measurements.

The DSP generates data in the above format at a rate of approximately 200 pulses per second.

## B. PRINCIPLES OF OPERATION

1. Position information. All position information is initially supplied in X-Y grid coordinates in nautical miles. Velocities are input in knots and direction of travel in degrees clockwise from North. The DSP converts this information to X-Y coordinates in yards relative to the IFM and



relative velocity components in the X and Y directions in yards per second. The relative velocity, Closest Point of Approach (CPA) and distance to CPA is calculated for all platforms.

2. Emitter input data consists of the transmit frequency in MHZ, pulse width in microseconds, PRI in milliseconds, transmitted power in KW, antenna gain in db, antenna beam width in degrees and antenna scan rate in seconds per revolution. DSP converts all input units to common units for computation.

3. IFM input data consists of the maximum and minimum frequencies of its pass band in MHZ, the minimum measurement time of the IFM in microseconds and the threshold sensitivity in db.

DSP utilizes the input data to calculate the received signal strength for each emitter as a function of range and the angle between the emitters antenna and the IFM platform. The maximum range of detection assuming maximum antenna gain is calculated and compared with the initial range and the CPA to determine when the emitter will come within range of the IFM, if ever. The pulse repetition cycle and antenna initial angle are assigned by assuming a uniform distribution of starting positions in these cycles and accessing a uniform distribution random number generator. When the emitter is within range, the portions of the antenna scan cycle that the antenna gain is high enough to allow detection are calculated.



On the basis of the above calculations, DSP stores the time of arrival at the IFM, counting transit times, for the first pulse of each emitter which will be received with a signal strength equal to or greater than the receiver sensitivity. These times are stored in an array which is then searched to find the next occurring time of arrival. As each pulse time of arrival becomes the next in the sequence of the receiver pulse train, DSP calculates the time of arrival of the next pulse from that emitter and stores that time in the array. Each time update continues to consider the transit antenna scan and the relative motion between the IFM and the emitter platform.

The DSP currently models the IFM with a 100% probability of detection of all pulses arriving with signal strengths equal to or greater than the threshold sensitivity. Additional coding can readily be added to provide a less than perfect detection scheme, false alarms, and an IFM directional antenna.

The DSP has been provided with selection indicators for selecting random variations to all emitter parameters. Coding has not been included to accomplish any such variation but can be readily added.

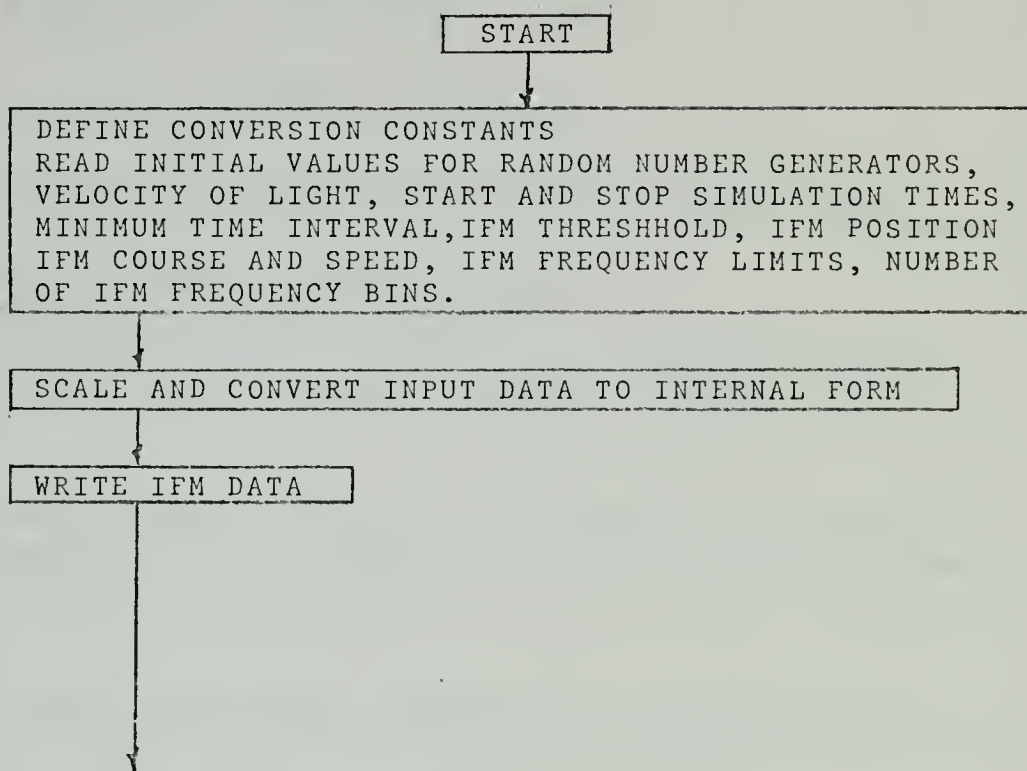
The DSP currently includes only two options for the emitter antenna scan type--steady and circular scans. Coding for additional scans can also be readily added.

The overall flow diagram for the DSP is shown in Figure 2.





# Data Simulation Program Flow Chart





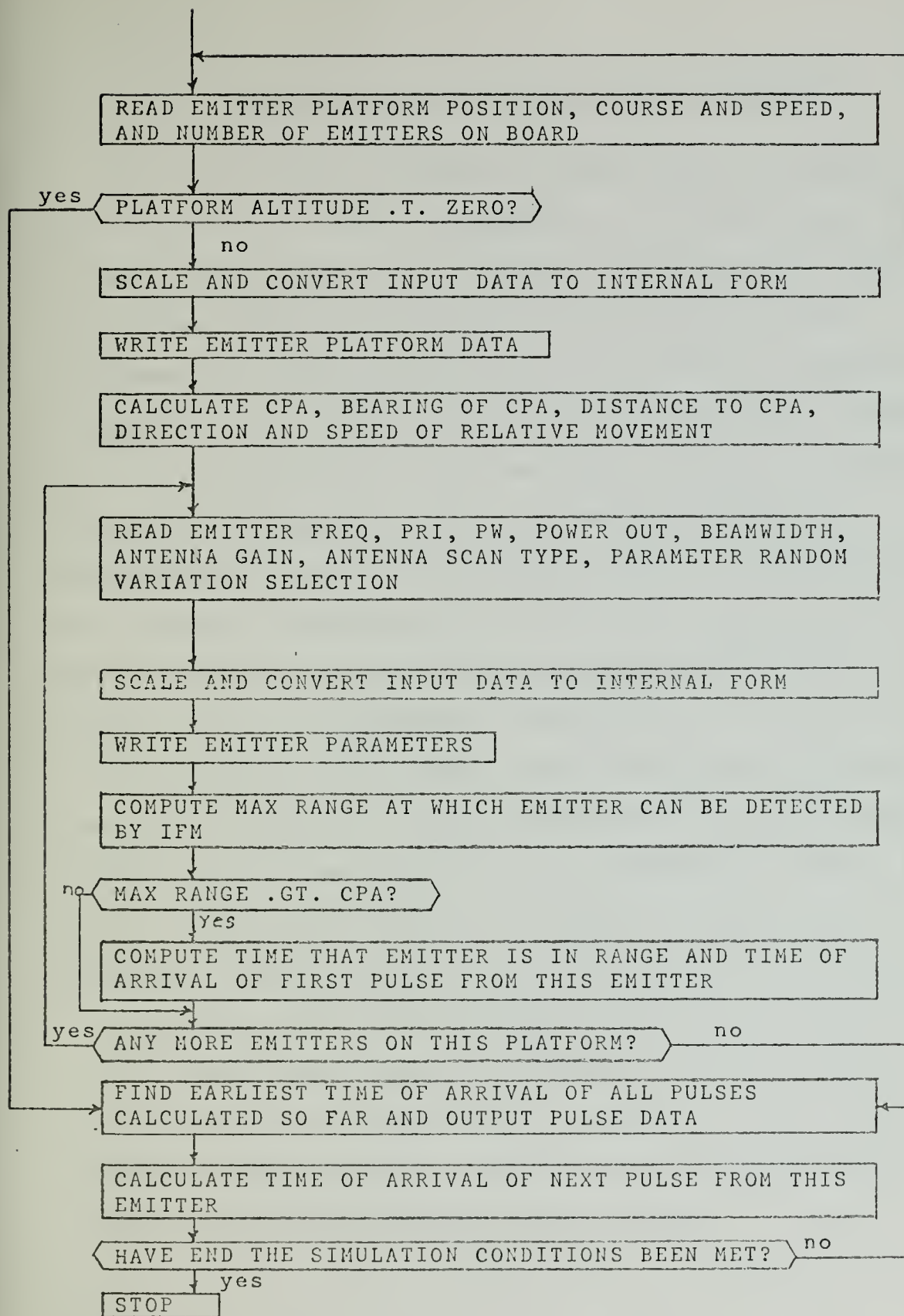


Figure 2. THE DSP ALGORITHM (SIMPLIFIED FLOW CHART)



## VI. OPTIMIZATION OF THE IFM DIGITAL PROCESSOR

The ATAC Assembly Language program listed in Appendix C and described in detail in Appendix D is written using the supplied instruction set. The major advantage of a microprogrammed computer is that the instruction set can be tailored for optimum efficiency in execution of a specific algorithm. Two primary results of this optimization are the saving of instruction fetch times when a series of instructions are microcoded and the time savings realized by performing operations simultaneously when the data paths do not overlap. Modifications to the instruction set are constrained only by the hardware configuration of the computer and the programmer's imagination.

In addition to the time savings associated with modifying the instruction set additional benefits can be accrued by modifying the hardware to allow simultaneous input and output operations, buffering the memory interfaces with high speed registers and instruction interleaving techniques.

Modifications of both microcode and computer hardware can be tested and evaluated by using the APSS Microprogramming Software. By simulating the desired microcode sequences, debugging and optimization efforts can be expended before a commitment to actual design change is made.



## A. MICROCODE SEQUENCES

Series of instructions which are shown to use a large percentage of the execution time of the program should be examined for microcoding first. The time expended by each instruction is output by the APSS Instruction Level Simulator in the form of a time histogram. An example of this histogram is shown in Appendix D. This histogram shows that the two instructions which use the most time during the execution of the program are the store data and load new data instructions. The program sequence which utilizes these instructions is required for every input pulse and is listed below.

Instruction	Purpose	Execution Time (microseconds)
STK DR,8,4	Store data	3.5
BRCS U, TOP	Branch to beginning	.8750
ADD IS,0,4	Increment address	.4375
RET DR,0,4	Fetch new data	3.5
LDR R,5,1	Move frequency word	.4375
BRCS Z, TOP	Test for presence of data	.4375
LDR IS,1,0	Put 0 in register 1	.4375
STR RX,1,0,1	Store a 0 in the data block	1.5625
ADD IS,0,4	Reset address pointer	.4375
LDR DX,6,EF,5	Fetch frequency file entry	1.3125
BRCS Z, STAR1	Test for a pulse train file	<u>.4375</u>
	Total time expended	13.8125

The average time expended per input data set during simulation runs was 45 microseconds. It is seen that 30%





of this time is spent in the store/fetch phase. This sequence placed in microcode would save an initial 4.3 microseconds in instruction fetch times. Additional savings are possible by the simultaneous incrementing of the address registers and simultaneous input and output operations as the input data and output data are using independent segments of memory. It is estimated that the execution time of the microcoded sequence would be approximately 6 microseconds which reduces the program execution time per pulse to approximately 40 microseconds. Additional microcode sequences can be developed, especially for the routine update data section of the program. A time saving of 30% is probable.

Using the technique of microcoding instruction sequences and optimizing the microprogram data flow, the average time per pulse can be reduced to 25 to 30 microseconds. This step alone increases the average pulse density capability of the system to 33K -40K pulses per second.

#### B. HARDWARE MODIFICATION

The time required to access and store the data can be reduced by a factor of four by altering the means of storing it. If the data is stored in four independent memory modules, parallel transfer of the four words is possible. A hardware modification is required to allow the computer to load four registers in parallel by supplying the additional data paths required.



Supplying an input data buffer and an output data buffer each of four words would allow loading the input buffer during execution of instruction sequences in the middle of the loop and then loading the working registers in parallel in one major cycle. For storing data, the buffer can be loaded in parallel in one major cycle and the data stored in memory from the buffer during execution of the remainder of the program. If two buffers are provided both the fetch and store operations can be conducted simultaneously. From the program's point of view, the execution time required for the 13.8 microsecond sequence of V.A above becomes .4375 microseconds.



## VII. FEASIBILITY ANALYSIS OF THE IFM DIGITAL PROCESSOR

Computer simulation of the IFM digital processor has been conducted. The algorithm presented in Chapter III was coded in ATAC Assembly language. The resultant program is described in Appendices C and D. The Data Simulation Program (DSP) was used to provide a realistic environment of received pulses in order to test the concepts presented in Chapters II and III. Sufficient time was not available to conduct simulation runs to test all conditions and to develop more than an initial evaluation of the concept's viability. A summary of results obtained, conclusions and recommendations for further study are included below.

### A. SUMMARY OF RESULTS

The ATAC computer was modelled as provided for in the APSS Instruction Level Simulator using the program described in detail in Appendix C. Due to limitations imposed by the Simulator, data was inserted into the ATAC constructive memory prior to the beginning of simulation. The data was prepared by the Data Simulation Program described in detail in Appendix D. A total of 1024 radar pulses were utilized in order to check on the accuracy of pulse train building, the development of PRI information and the average time required to handle each pulse. The results of the simulation were the completely accurate discrimination of pulses by frequency and pulse width and the calculation of



the correct PRI in all cases. The total time required for the ATAC to process 1024 pulses was 0.046 seconds or an average of 45 microseconds per pulse. The results are summarized in the table below.

#### Simulation input data.

Number of radar emitters	9
Total number of pulses utilized	1024
Total real time simulated	0.1568 sec

#### Simulation results.

Accuracy of pulse association	100%
Total ATAC simulated computer time	0.046 sec
Average time per pulse	45 microsec
Maximum average data rate possible	22,000 pps

### B. CONCLUSIONS

The simulation was conducted with stable pulse widths and PRI. Even so, on the basis of the results of the simulation and on the information contained in Chapter V, it is feasible to construct a system capable of significant amounts of automatic signal classification in a high density environment with the average rate of information in the bandwidth of an IFM in the range of 25K to 50K pulses per second.

### C. RECOMMENDATIONS

Based on the results of this study, the following recommendations for further study are submitted.





1. Continue simulating the high density environment with the programs listed in Appendices C and D adding to the complexity of the input data in order to determine the optimum algorithm for the solution of the problem.

2. Use the results of the simulations to develop additional special purpose instructions which optimize execution of the programmed algorithm.

3. Use the results of the simulations to develop desirable hardware reconfigurations which will optimize the execution of the programmed algorithm.

4. Use the features provided in APSS to test and evaluate the newly developed hardware configuration and instruction set.

5. Expand the basic procedures outlined herein to other fields that encounter high data rates and require automatic data processing. Examples are radar systems, communications systems and sonar systems. The desirability of specifically designed processing equipment has been demonstrated.

Current technology is producing these processors which eliminate the processing time and price penalties paid when utilizing general purpose digital computers.



## APPENDIX A

### INSTALLATION OF THE ATAC PROGRAMMING SUPPORT SYSTEM (APSS) AT THE NAVAL POSTGRADUATE SCHOOL

--The ATAC Programming Support System operates on a local or remote IBM 360/370...

ATAC Principles of Operation (Volume 1)

--If something can possibly go wrong, it will...

Murphy's First Law of Dynamics

A. Installation of the ATAC Programming Support System on the IBM 360/67 Operating System at the Naval Postgraduate School by the author was required in order to allow programming of algorithms in an actual representative machine assembly language and to determine execution times and overload points for the algorithm/computer team in an EW environment. After negotiations with ATI Corporation, arrangements were made for a tape copy of the portions of APSS required to conduct instruction level simulations. This tape was received on 10 May 1974. The ensuing events are presented as an example of interfacing problems that can be encountered. Problems encountered during the program implementation are listed in the order of their occurrence along with the corrective action taken.

#### 1. Tape density.

a. The original tape was prepared by ATI using a remote terminal to an IBM 370 installation. This tape was



taken to NPS by the author and an attempt was made to copy from the tape. The tape simply ran out indicating that the Operating System was unable to find any of the specified files on the tape. A utility program 'TAPEOUT' was used to determine what, if anything was on the tape. According to the utility program output there was nothing understandable recorded on the tape at all. A belated investigation of the JCL instructions that produced the tape revealed that it had been prepared on a dual density tape unit and recorded with a density of 1600 bits per inch. The installation at NPS does not support recording densities of greater than 800 bpi.

b. Corrective action. A second tape was generated by ATI specifically recorded at 800 bpi. This tape was picked up by the author on 14 May 1974.

## 2. Block length.

a. Files 1 and 2 of the new tape were successfully read by the NPS computer. These files contained instructions on how to access File 3 which contained the Instruction Level Simulator in object module form. The required steps were:

- 1) Copy the object modules from the tape onto a direct access storage device such as a disk pack.

- 2) Build an absolute load module by providing local linking data between the various portions of the program contained in the object modules. In object module form, the program consists of a group of subroutines which



are stored with instruction and data locations specified as relative to the individual subroutines start point. Building a load module orders these individual sub programs and establishes a common relative base address so that when this entry point is specified (when loading the program for execution) the instruction sequence proceeds as originally designed, including linking between these sub programs.

### 3) Load and execute the APSS Simulator.

Step 1 was accomplished. However, when attempting to access the file created by copying the tape, the computer was unable to identify the contents of the file and returned the error message 'Permanent I/O Error on Attempting to read File Headings'. Investigation indicated that this could be caused by an incompatible block length of the original object modules. Due to size limitations and buffering considerations, records (data) transferred by computers are organized into blocks of data. These blocks are identified by length and where the next sequential block of data is to be found. To make sense to a computer, when the data consists of an executable program, it must be reassembled with the same block structure in the proper alignment that it had when the program was assembled. Investigation revealed that the original assembly of the program was conducted using a 3330 disk pack and was created with a block length of 13K bytes. The maximum block length supportable at NPS is 7K bytes using a 2314 disk pack. This meant that the NPS





computer could not find the beginning of the second and subsequent data blocks containing the program.

b. Corrective action. When finally diagnosed, this problem was corrected by specifying a track overflow option. This option allows data blocks to 'spill over' onto adjacent tracks of the 2314 disk pack. Use of this feature is dangerous in that the data overflows onto the adjacent track no matter who the adjacent track belongs to or what it contains. This requires using a disk pack with enough room on it so that the entire program can be assigned contiguous tracks.

### 3. Incompatible instructions.

a. By using the track overflow option, the program was successfully copied into temporary direct access storage and a load module was created using standard IBM supplied utility programs. At this point the program was in executable form. The first attempt to use the program was made using a bench mark program supplied by ATI which was to be used to ensure proper operation. When this program was loaded, the object deck was assembled properly. However, when the simulation itself was attempted, the NPS computer promptly quit and listed an error message which in idiomatic translation means 'I don't understand what you are telling me to do and so I quit'. A dump of the core locations containing the offending instruction revealed the presence of a number of instructions which were implemented for the IBM 370 and are not executable (understandable to) by an IBM 360.



Communication with ATI disclosed that the affected portion of the Simulation Program was written in IBM 370 Assembly Language and that there were ten of these instructions. After further investigation by the author, a similar 360 instruction was selected that was presumed to operate properly for the majority of cases. This new instruction word was placed in the ten locations using a local utility program. On completion, the bench mark program was successfully executed and comparison with the version run at ATI showed that identical results were obtained.



## APPENDIX B

### INSTRUCTIONS FOR USE OF THE APSS INSTRUCTION LEVEL SIMULATOR ON THE IBM 360/67 OPERATING SYSTEM AT THE NAVAL POSTGRADUATE SCHOOL

A. For general and detailed information on how to use the IBM 360/67 OS, the reader is referred to the W. R. CHURCH COMPUTER CENTER USER'S MANUAL.

The ATAC Programming Support System Instruction Level Simulator currently resides in load module form on Cell 5 of the 2321 Data Cell under file name S1434.PDF.APSS. The steps recommended for use of this program are:

1. Write any desired program in ATAC Assembly Language following the directions of ATAC PRINCIPLES OF OPERATION (VOLUME I).

2. Include desired simulated Input/Output operations following the directions of ATAC APSS INSTRUCTION SIMULATOR (VOLUME 2, Section IV). For this purpose it may be necessary to replace supplied FORTRAN dummy subroutines with subroutines written to simulate data generation and interrupt timing. The Job Control Language sequence required to accomplish this replacement is shown in paragraph C.

3. Include desired Simulator Control instructions following the directions of ATAC APSS INSTRUCTION SIMULATOR (VOLUME 2, Section IV).



4. Prepare the coded version of 1, 2, and 3 above following the directions of ATAC APSS ASSEMBLER/LOADER (VOLUME 2, Section III) for precise card formats.

5. Construct the input card deck for the desired job including required control features in accordance with ATAC APSS JOB MANAGEMENT (VOLUME 2, Section I).

On completion of 1 through 5, the user will have a card deck the first card of which is \$JOB and the last card is \$END. The following IBM JCL cards are required in order to execute the program.

```
// (STANDARD JOB CARD. SEE USER'S MANUAL)
// TEST EXEC PGM=APPS,REGION=250K
// STEPLIB DD DSN=S1434.PDF.APSS,UNIT=2321,
//     DISP=(OLD,KEEP),VOL=SER=CEL005,DCB=BLKSIZE=400
// FT06F001 DD SYSOUT=A,DCB=(RECFM=FBA,LRECL=133,
//     BLKSIZE=3325)
// FT05F001 DD DDNAME=SYSIN
// FT08F001 DD UNIT=SYSDA,SPACE=(CYL,1)
// FT09F001 DD UNIT=SYSDA,SPACE=(CYL,(7,2)),
//     DCB=(RECFM=VBS,BLKSIZE=7180,LRECL=92)
// FT10F001 DD UNIT=SYSDA,SPACE=(CYL,(7,2)),
//     DCB=(RECFM=VBS,BLKSIZE=4204,LRECL=42,BUFNO=1)
// FT20F001 DD UNIT=SYSDA,SPACE=(CYL,(7,2)),
//     DCB=(BUFNO=1,RECFM=VBS,BLKSIZE=2004,LRECL=500)
// SYSPRINT DD SYSOUT=A,DCB=(RECFM=FBA,LRECL=133,
//     BLKSIZE=3325)
// SYSIN DD *
```

\$JOB

.  
.  
.  
APSS PROGRAM

.  
.  
.  
\$END  
/\*





B. The source tape for the APSS Instruction level simulator is stored at the W. R. CHURCH COMPUTER CENTER under the name 'ATI.105'. Files 1 and 2 on this tape contain instructions for the use of the entire APSS system. The instructions given are not in general applicable for use and retrieving these files is not considered desirable. If retrieval is warranted, use the IBM utility program IEBGENER. For further information refer to the USER'S MANUAL.

File 3 contains the object module form of the APSS Instruction Level Simulator. The following steps are required to prepare it for use in the event of failure to the Data Cell. All of these steps may be accomplished in one JOB if desired. The total CPU time required is approximately 10 seconds.

1. Move the object modules from the tape to disk storage. ENSURE the actual disk pack used has sufficient unallocated room for contiguous assignment of tracks. The object module file has a block length of 13K bytes and the track overflow feature has to be selected in order to be able to access the new disk file successfully. The track overflow feature allows data blocks to overflow from one track onto the adjacent track, whether it is assigned to you or not. The normally used USER disks will not usually have sufficient space available. Special arrangements should be made before the file is moved. The required JCL statements are as follows.



```

// (STANDARD JOB CARD)
// EXEC PGM=IEHMOVE,REGION=150K
// SYSPRINT DD SYSOUT=A
// SYSUT1 DD UNIT=SYSDA,SPACE=(TRK,(40),,CONTIG)
(1) // DA1 DD UNIT=2314,DSN=S1434.ATI.PDF1,SPACE=(TRK,
//      (80,10,10),,CONTIG),
(2) //      DCB=RECFM=T,
//      DISP=(NEW,KEEP),VCL=SER=PAT003,
//      LABEL=RETPD=060
// T1TAPE DD UNIT=(2400,,DEFER),DISP=NEW,PASS),
//      LABEL=(3,SL,,IN), DCB=(DEN=2,BLKSIZE=800,
//      LRECL=80,RECFM=FB),VOL=SER=ATI105,
//      DSN=ATI.TEMP.APSS1
// SYSIN DD *
(3) COPY PDS=ATI.TEMP.APSS1,TO=2314=PAT003,FROMDD=T1TAPE,
      TODD=DA1, FROM=2400=(ATI105,3),
      RENAME=S1434.ATI.PDF1
/ *
```

Note 1: File names selected must be consistent throughout.

Note 2: This selects the track overflow option.

Note 3: The asterisk (\*) in column 72 is required as an indication that another card follows which is a continuation of the COPY PDS card.

2. The object modules now on the disk must be built into a load module and stored in a permanent file. The Data Cell is adequate for this purpose. The following JCL cards will accomplish this step.

```

// BUILD EXEC PGM=IEWL,REGION=100K,PARM='OVLY,
//      XREF,LET,LIST'
// SYSPRINT DD SYSOUT=A
// LIBRARY DD DSN=S1434.ATI.PDF1,UNIT=2314,
//      VOL=SER=PAT003,DISP=SHR
// SYSLIB DD DSNAME=SYS1.FORTLIB,DISP=SHR
// SYSLMOD DD DSNAME=S1434.PDF.APSS,UNIT=2321,
//      VOL=SER=CEL005, DISP=(NEW,KEEP),
//      LABEL=RETPD=060,
//      SPACE=(TRK,(300,20,2),RLSE)
```



```

// SYSUT1 DD UNIT=SYSDA,SPACE=(TRK,(19,19)),,
//      CONTIG),SEP=SYSLMOD
// SYSLIN DD *
INCLUDE LIBRARY (PMUDL)
CHANGE MSIM(IHESAPD)
INCLUDE LIBRARY (LIBR2)
INCLUDE LIBRARY (ATACIO)
INCLUDE LIBRARY (MSIM4,ASEM5,SIMU11,SIMTR1,SIMIO1,GUL)
INCLUDE LIBRARY (XPLMON)
OVERLAY A1
INSERT MSIMUL,*MSIMULA,IHENTRY,IHESAP
INSERT MINT,IN,OUT
INSERT IHEDBN,IHEXID
INSERT IHEBSM,IHECSM
INSERT IHEBSK, IHEIOX, IHEIOP, IHEDID, IHEDOB
INSERT IHEDIB, IHEDOA, IHEIOB
INSERT IHEIOA, IHEOCL
INSERT IHEBSD, IHEBSF
INSERT IHEJXS
INSERT IHEOSD, IHEOST, IHEBSI
INSERT IHEVPF, IHEDMA, IHEVFB
INSERT IHEDNC, IHEVFD, IHEVFA, IHEVPD, IHEVPB, IHEVSC
INSERT IHEVSD, IHEVFE, IHEDCN, IHEUPB
INSERT IHEVFC, IHEVPE, IHEVPG, IHEVQB, IHEVQC
INSERT IHEABN, IHEIOD, IHEIOF, IHEPRT, IHEVQA, IHESPRT
INSERT IHEBEG, IHEERR, IHESIZ
INSERT MISET
OVERLAY A1
INSERT ASSEM, REWIND,REW72,DSKOUT,CARDIN,DISKIN,
      ERPRT,PRIADD
INSERT WRDATA,PRICOM,PRINOR,WRITEX,REFTIT,PREF,ERTIT
OVERLAY A1
INSERT PARMRD, PRESIM
OVERLAY A1
INSERT SMLTR,NRMTRM,STRTSM,TPAGE
INSERT RDCRD,ABNRMT,ARTHFP,TRACE,HGRAM,HGRAMI,HGRAMS
INSERT IOINIT,ACTIVE,SIMTIM
INSERT DEVDTA,ACT,PRGTIM,RAND,TIME,INT,RAND,DEADT,DEBUG
OVERLAY A2
INSERT LEVEL,IOR,SPLIT,DMAIOI,DMAIOA,DMAIOD,RIOIO
INSERT REMACT,DMA,DMATM,RIO,RIOTM,RIOINT,INTOLY,DMAINT
INSERT DTRAN,PUTACT,RANDOM
OVERLAY A1
INSERT HGPRNT
OVERLAY A1
INSERT LOADER
OVERLAY A1
INSERT LINK,ENTEXT,SLLH
OVERLAY A1
INSERT PLATAC,IOPACK
OVERLAY $OBJECT(REGION)

```



```

INSERT OBJECT,INIT,LIB,RCALPH,RCHEX,RCINT
INSERT MDATE
OVERLAY $DUMP(REGION)
INSERT SMDUMP,PAGE
ENTRY MAIN
      NAME APSS

```

/ \*

3. When the load modules have been built onto the Data Cell, the disk file is no longer required and should be scratched. The following JCL, cards will accomplish this.

```

// EXEC PGM=IEHPRGM
// DD1 DD DISP=(OLD,DELETE),UNIT=2314,VOL=SER=PAT003
// SYSPRINT DD SYSOUT=A
// STSIN DD *
      SCRATCH DSNAME=S1434.ATI.PDF1

```

/ \*

4. At this point, the load module is on the Data Cell but there are 11 memory locations which are required to be individually changed in order for the program to execute. See APPENDIX A for detailed reasons why. Changing the memory locations requires the use of a utility program which is under close control of the Computer Center personnel for obvious reasons. The locations, current contents and required new contents are listed below. For assistance in making this change, see the Director of Operations at the Computer Center.

All numbers are hexadecimal

NAME APSS SMLTR

Location	Old Contents	New Contents
115E	BD53	4950
1166	BD53	4950





Location	Old Contents	New Contents
1176	BD53	4950
117E	BD53	4950
118E	BD53	4950
1196	BD53	4950
11A2	BD53	4950
1200	BD53	4950
1208	BD53	4950
1214	BD53	4950
13B2	A5EC	B39B

5. The APSS Instruction Level Simulator is now ready for use.

C. A subroutine may be substituted for any of the dummy Input/Output subroutines supplied very simply. The first step is to write and debug the new subroutine. Care must be taken to ensure that the new subroutine has the same name and identical calling arguments as the old one. Once the subroutine is fully ready for use, it may replace the original one as shown below. It must be pointed out that once this step is accomplished, the only way to retrieve the original subroutine is to build the entire system over again.

```
// (STANDARD JOB CARD)
```

```
// EXEC FORTCL
```

```
// FORT.SYSIN DD *
```

```
(FORTRAN SOURCE DECK)
```

```
/ *
```



```
// LINK.SYSLMOD DD DSN= S1434.PDF.PASS,DISP=(OLD,KEEP),  
// UNIT =2321,VOL=SER=CEL005  
// LINK.SYSIN DD *  
NAME (SUBROUTINE NAME) (R)
```



## APPENDIX C

### THE IFM DIGITAL PROCESSOR PROGRAM LISTING

The IFM Digital Processor Program (IDPP) is the implementation of the algorithm presented in Chapter III in ATAC Assembly Language. For ease in examination of the coding used, a listing of the instructions used in this program and their functions is included in Appendix E.

1. Program Listing. The program is listed by the APSS Assembler and provides the following information.

a. Column 1. The first column lists the instruction location relative to the start of the program in hexadecimal. The program actual entry address is location 10 so that in the simulator output listings, locations appear  $10_{16}$  higher than they do on the program listing.

b. Columns 2. The second and third columns contain the actual hexadecimal contents of the instruction locations. Single word instructions do not have an entry in the third column.

c. The image of the input program cards is reproduced. Lines that have a period occurring as the first entry are comment cards.

d. The sequence number of the cards is simply the order in which they occurred in the data stream.

2. The program has been written as one entity in order to save linking by subroutines and paying the associated time



overhead. The different functions of the program have been separated by blank comment cards for ease of reference. The basic function of each instruction has been included in the comments made in the margin adjacent to the instruction.

3. Beginning with the location HADRS, the following cards establish data storage requirements and represent the only means of interpreting the results of the simulation. The Simulator automatically dumps the entire ATAC core storage on completion of the simulation. By referencing the locations of the various variables and data, the contents at the completion of the simulation run may be determined. A summary of the meaning of the data storage locations is given below.

Variable	Interpretation
HADRS	Used to specify limits of the instruction versus time Histogram
TRACK	The output pulse train file. Individual files begin every $10_{16}$ locations. Interpretation of the word values is contained in Section III.C.1,2,3.
EFILE	Frequency input file. The contents of EFILE locations show the mapping conducted from frequency information to the proper pulse trains.
TFILE	The contact file entry file. Locations correspond to the pulse train file and are in the same order. The contents of even





Variable	Interpretation
	words of the file contain the entry location of the corresponding pulse train file.
OFLO	The overflow storage area.
OFLOW	Variable used to point to the next available location in the overflow area.
NEXTF	Variable used to point to the last pulse train file activated.
PFILE	Used to define the extent of TFILE for the purposes of initializing the TFILE locations to the proper value by reading in data cards.
DATA	Locations used to store input pulse data.
DATAR	Used to define the extent of DATA for the purposes of initializing the DATA locations to the data values by reading in data cards.

#### 4. The simulator output.

a. A print of the contents of each of the 16 general registers, the condition code register, the input/output interrupt masks and the simulated computer time elapsed since the beginning of the simulation can be provided. This print out must be specifically requested with a Trace request. It is turned on and off within the program to avoid a line of output for each and every instruction executed by the simulated computer. The feature is very useful for checking the program flow.



b. The simulation histogram of time expended by the instructions at each real location (10 + the program listing location). This feature shows which instructions take more time in execution than others. By noting which instructions or instruction sequences take abnormal amounts of time, the program flow can be changed to improve the overall efficiency. Additionally this output shows those instructions which should be looked at with the possibility of redefining a new microcode instruction or modifying the hardware configuration in order to improve the time required for execution of the program.

c. Core dump. This output is the primary means of verifying proper operation of the program. Variable locations in the program listing are given in actual core locations if the variable is in Random Access Memory (RAM) or Read Mostly Memory (RMM).













IFM	LOC	OBJECT CODE	CARD IMAGE	TIME: 17:10:23	06/16/74	PAGE	CARONUM
0047	E206	1A01	ANDT	GET LAST FILE USED	IFM1070	108	
0048	E207			SET VALUE FOR NEXT FILE	IFM1080	109	
0049	E208			NEXT FILE ADDR	IFM1090	110	
0050	E209	1981		GET FILE ADDR ADDRESS	IFM1100	111	
0051	E210			IF FILE BUSY, GET THE NEXT ONE	IFM1110	112	
0052	E211	1A01		STORE FILE ADDR FOR NEXT FILE	IFM1120	113	
0053	E212	1981		STORE FREQUENCY IN CONTACT FILE	IFM1130	114	
0054	E213			LCAL PT FILE ENTRY A00	IFM1140	115	
0055	E214	1981		STORE PT FILE LINK	IFM1150	116	
0056	E215	1800		PUT INITIAL FILE VALUES IN REG 9-12	IFM1160	117	
0057	E216			SET FILE CTR VALUE IN PRI WORK	IFM1170	118	
0058	E217			LOAD TOA	IFM1180	119	
0059	E218			STORE FILE ENTRY	IFM1190	120	
0060	E219			GC GET NEXT PULSE	IFM1200	121	
0061	E220			GET THE ADDRESS OF THE NEXT FILE	IFM1210	122	
0062	E221			IF NO NEXT FILE, START ONE	IFM1220	123	
0063	E222			SET REL ADDRESS OF NEXT FILE	IFM1230	124	
0064	E223			GO TRY THE NEXT FILE	IFM1240	125	
0065	E224			FIND THE NEXT OVERFLOW LOCATION	IFM1250	126	
0066	E225			PREPARE THE LINKING WORD	IFM1260	127	
0067	E226			LINKING ADDRESS	IFM1270	128	
0068	E227			STORE LINKING WORD	IFM1280	129	
0069	E228			SET REL ADDRESS OF NEXT FILE	IFM1290	130	
0070	E229			INCREMENT OVERFLOW LOCATION	IFM1300	131	
0071	E230			STORE NEXT OVERFLOW LOCATION	IFM1310	132	
0072	E231			GO START THE REST OF THE FILE	IFM1320	133	
0073	E232			A00 ONE TO PULSE COUNTER IN REG 10	IFM1330	134	
0074	E233			IF ZEROC, BRANCH TO CALCULATE PRI	IFM1340	135	
0075	E234			STORE PULSE COUNTER	IFM1350	136	
0076	E235			CALCULATE WHERE DATA BELONGS	IFM1360	137	
0077	E236			DATAS REL A00RES	IFM1370	138	
0078	E237			PUT INTO REG 5	IFM1380	139	
0079	E238			A00R CF THE PREVIOUS TIME	IFM1390	140	
0080	E239			FETCH PREVIOUS TIME	IFM1400	141	
0081	E240			CALCULATE THE TIME DIFFERENCE	IFM1410	142	
0082	E241			IF PULSE OUT OF SEQ, DISREGARD	IFM1420	143	
0083	E242			IF TIME DIFFERENCE .GT. .8 SEC	IFM1430	144	
0084	E243			ZERO TIME DIFFERENCE	IFM1440	145	
0085	E244			LOAD DATA(PRI)	IFM1450	146	
0086	E245				IFM1460	147	
0087	E246				IFM1470	148	
0088	E247				IFM1480	149	
0089	E248				IFM1490	150	
0090	E249				IFM1500	151	
0091	E250				IFM1510	152	
0092	E251				IFM1520	153	
0093	E252				IFM1530	154	
0094	E253				IFM1540	155	
0095	E254				IFM1550	156	
0096	E255				IFM1560	157	
0097	E256				IFM1570	158	
0098	E257				IFM1580	159	
0099	E258				IFM1590	160	





















ATAC INSTRUCTION LEVEL SIMULATION																							
PC	INSTRUCTION	OPER	R0	R1	R2	R3	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	CCR	IMR	ITR	TOT	TIME
005C	DX,5,1981,6	0029	.	.	.	.	.	.	0005	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	63.9
005E	IS,6,0001,6	1080	.	.	.	.	.	.	.	1080	.	.	.	.	.	.	.	.	.	1	00000000	00000000	64.4
005F	OX,6,1800,7	0005	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	66.3
0060	IS,9,4,FF0	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	68.7
0061	IS,11,2,3	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	68.7
0062	IS,12,3	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	69.1
0063	IS,13,4	0009	.	.	.	.	.	.	.	1084	.	.	.	.	.	.	.	.	.	2	00000000	00000000	69.1
0064	IS,14,5	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	70.4
0065	IS,15,6	1A10	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	70.4
0066	IS,16,7	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	71.5
0067	IS,17,8	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	71.5
0068	IS,18,9	0045	1A0C	0045	10E1	.	0007	0045	.	.	.	.	.	.	.	.	.	FFFE	.	4	00000000	00000000	76.5
0069	IS,19,10	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	77.4
0070	IS,20,11	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	77.4
0071	IS,21,12	0000	1A10	.	.	.	.	.	.	0045	.	.	.	.	.	.	.	.	.	4	00000000	00000000	82.3
0072	IS,22,13	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	82.3
0073	IS,23,14	0004	.	.	.	.	.	.	0004	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	83.7
0074	IS,24,15	0006	.	.	.	.	.	.	0006	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	83.7
0075	IS,25,16	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	85.1
0076	IS,26,17	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	85.1
0077	IS,27,18	0000	.	.	.	.	.	.	.	0000	.	.	.	.	.	.	.	.	.	1	00000000	00000000	86.1
0078	IS,28,19	0004	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	86.1
0079	IS,29,20	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	88.4
0080	IS,30,21	0006	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	88.4
0081	IS,31,22	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	89.4
0082	IS,32,23	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	89.4
0083	IS,33,24	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	90.3
0084	IS,34,25	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	92.8
0085	IS,35,26	10C0	.	.	.	.	.	.	.	10C0	.	.	.	.	.	.	.	.	.	1	00000000	00000000	92.8
0086	IS,36,27	0007	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	94.8
0087	IS,37,28	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	94.8
0088	IS,38,29	0007	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	97.4
0089	IS,39,30	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	97.4
0090	IS,40,31	1A14	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	103.7
0091	IS,41,32	0010	1A10	0010	24E9	.	0028	0010	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	103.7
0092	IS,42,33	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	104.6
0093	IS,43,34	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	104.6
0094	IS,44,35	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	105.4
0095	IS,45,36	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	105.4
0096	IS,46,37	0000	1A14	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	110.8
0097	IS,47,38	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	110.8
0098	IS,48,39	0000	1A10	0010	24E9	.	0028	0010	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	111.2
0099	IS,49,40	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	112.8
0100	IS,50,41	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	112.8
0101	IS,51,42	0000	1A14	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	117.8
0102	IS,52,43	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	117.8
0103	IS,53,44	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	119.1
0104	IS,54,45	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	119.1
0105	IS,55,46	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	121.6
0106	IS,56,47	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	121.6
0107	IS,57,48	0006	.	.	.	.	.	.	0006	.	.	.	.	.	.	.	.	.	.	4	00000000	00000000	123.5
0108	IS,58,49	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	123.5
0109	IS,59,50	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	125.7
0110	IS,60,51	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	125.7
0111	IS,61,52	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	128.8
0112	IS,62,53	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	2	00000000	00000000	128.8
0113	IS,63,54	0000	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	.	1	00000000	00000000	130.1



ATAC INSTRUCTION LEVEL SIMULATION										DATE 06/16/74	TIME 17:11:01	PAGE 1											
PC	INSTRUCTION	OPER	R0	R1	R2	R3	R4	P5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	CCR	IMR1	ITR	TOT TIME	
0021	SIM 5,0000		2A04	0003	340E	0000	0000	0035	FFFF	0000	1244	0004	0013	340E	0000	0000	0013	0000					
0023	SIM 7,0000		2A04	0003	340E	0000	0000	0035	FFFF	0000	1244	0004	0013	340E	0000	0000	0013	0000					
***** NORMAL TERMINATION AT 0023																							
																				00000000	00000000	46246.9	
																				00000000	00000000	46246.9	



[illegible]





DATE 06/16/74 TIME 17:12:44 PAGE 2  
\* = 6.00E-05 = 3.00E-05  
4.2E-03 4.8E-03 5.4E-03 6.0E-03







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## APPENDIX D

# THE IFM DIGITAL PROCESSOR PROGRAM DETAILED DESCRIPTION

## A. PROGRAMMING

The coding used for the ATAC Assembly Language Program was developed by encoding each block of the algorithm flow chart of Figure 1 separately and then linking the blocks together. These coding blocks are described below.

1. LOAD DATA FROM DATA STORAGE. The data loading operation is critical in that it requires considerable execution time and is required for every pulse. The most efficient load instruction is the RETURN which is designed to return stacked values. This instruction automatically fetches a sequence of words and decrements the address pointer. In using this instruction in this application, prior and post operations to the address pointer are required in order to keep the pointer at the proper location. The sequence required is as follows. The actual instructions are indicated.

TOP    ADD IS,0,4    Add 4 to the address pointer in  
                      register 0.

ADD IS,15,1      Increment Program Control Pulse Counter

```
BRCS  Z,DONE      Go stop simulation if enough pulses
                  have been analyzed.
```





RET DR,0,4            Starting at the address in register 0 decrement the address and fetch the contents of the address. Repeat until 4 values have been fetched. The returned values are stored in registers 1-4 in the order they appear in memory. On completion of the operation, the address pointer value is 4 less than at the beginning.

2. DATA AVAILABLE? To test the contents of register 1 an operation has to be performed to set the condition code register. The operation selected is to move the contents to register 5 for future operations. Register 1 will later be used as a general zero contents and indexing register.

LDR R,5,1            Load the contents of register 1 into register 5.

BRCS Z,TOP           If the contents of register 5 (frequency) are zero, branch to the beginning (TOP) and access the same data block again. This sets up the no input data idle loop.

3. ZERO DATA LOCATIONS, INCREMENT ADDRESS POINTER. The frequency word location in the data memory is set to zero indicating the data for that pulse has been read. The address



pointer in register 0 is incremented to point at the location of the data words of the next pulse.

LDR	IS,1,0	Load 0 into register 1
STR	RX,1,0,1	Store the contents of register 1 in the location whose address is the sum of registers 0 and 1.
ADD	IS,0,4	Add 4 to the contents of register 0.
		Set the data file pointer for the next pulse.

4. FIND CONTACT FILE NUMBER. The frequency word in register 5 is used as a relative address for entry into the frequency file. The frequency word is copied into register 7 so that it can be saved in the event multiple files exist for this frequency.

LDR	R,7,5	Load the contents of register 5 into register 7.
FLINK LDR	DX,6,EFILE,7	Load register 6 with the contents of the location whose address is the sum of EFILE, the base address of the frequency file, and register 7.

5. FILE EXISTS? If no file for this frequency has been established, the contents of the frequency file is 0. A branch on condition zero instruction is used.

BRCS	Z,STAR1	If frequency word is zero, branch to STAR1 where a file will be created.
------	---------	--

6. FIND CONTACT FILE ENTRY ADDRESS. This instruction is executed only if the frequency file already exists. The



lower byte of the frequency file entry is the relative address of the proper contact file entry. This file has two words, the second word is the pulse train file entry address. The coding to achieve the linking is shown below. At the start of the sequence, the frequency file contents are in register 6.

```
LDLB R,14,6      Load the lower byte of register 6  
                  into register 14
```

```
LDR DX,8,TFILE,14 Load register 8 with the contents  
                  of the address formed by adding the  
                  contents of register 14 and the value  
                  of TFILE.
```

7. PW = FILE PW? The most efficient coding of this algorithm step depends on the relative frequency that the condition is met. If the average condition is that the incoming pulse width at this point will be equal to the file pulse width, the most efficient coding will return the first two words of the pulse train file together. If the branch is to be taken, the most efficient coding will return just the single pulse width word. The latter condition was chosen. Using the entry address contained in register 8, the first pulse width of the file is returned, compared to the incoming pulse width and the appropriate branch taken. The ATAC instruction set contains a compare between limits instruction which would perform the desired operation but it does not have a mode that is compatible with the program. The use of the ATAC instruction requires



enough manipulation of the contents of registers so that it requires more execution time than directly coding the individual steps. The coding for this operation is as follows.

LDR RX,9,1,8	Load register 9 with the contents of the address formed by adding register 8 and register 1 (register 1 still is 0)
LDR R,13,9	Load register 13 with the contents of register 9, This is done to eliminate the requirements to load register 9 again.
SUB R,13,4	Subtract the contents of register 4 (incoming pulse width) from the contents of register 13 and place the results in register 13.
BRCS P,TEST	If the result is positive branch to the positive test (skip the following instruction).
LAC R,13,13	Load the arithmetic complement of register 13 into register 13.
TEST CMP IS,13,4	Compare the magnitude of the pulse width difference in register 13 with the threshold value 4.
BRCS P, NTRY	If the contents of register 13 is greater than 4, the branch is taken to location NTRY which is the address of the beginning of the LOOK FOR NEXT FILE routine.





8. HAS PRI BEEN CALCULATED? The contents of the location following the pulse width word in the pulse train file is the PRI control word. If its contents are positive, a PRI has been calculated for the pulse train and the contents of the word is the value of the PRI. If the contents of the word is 0, the pulse train has an unstable PRI. In both of these cases, the program should proceed to update the pulse train file data. If the contents of the PRI word are less than zero, the pulse train file is still building and the program should proceed to the build file routine.

ADD IS,1,1      Add 1 to the contents of register 1.  
Register 1 will be used as an index  
to step to the next word in the pulse  
train file.

LDR RX,10,1,8    Load register 10 with the contents of  
the address formed by adding the con-  
tents of registers 1 and 8.

BRCS N,BUILD      Branch to the beginning of the build  
file routine if the contents of  
register 10 are negative.

9. TIME SINCE LAST PULSE LARGE? The UPDATE routine now calculates data to be used to update the pulse train file. This first operation requires the return of the next two words of the pulse train file which contain the time that the last update occurred. The difference between the last update time and the current pulse time of arrival contained in registers 3 and 4 is used to determine whether the



PRI will be updated or SPR calculated. The test used is whether the upper half of the double precision difference of the two times of arrival is zero. This results in the algorithm considering all time intervals greater than 0.8 seconds as SPR and all intervals less than 0.8 seconds as PRI.

UPDATE	ADD	IS,1,1	Step the indexing register to fetch the next word
	LDR	RX,11,1,8	Load the lower half of the time word into register 11
	ADD	IS,1,1	Step the index register again
	LDR	RX,12,1,8	Load the upper half of the time word into register 12
	LDR	R,6,2	Load the contents of register 2 into register 6
	LDR	R,7,3	Load the contents of register 3 into register 7. These two instructions copy the double precision new time into registers 6 and 7 so that the actual time value is retained in registers 2 and 3
	DSUB	R,6,11	Double precision subtract the contents of registers 11 and 12 from the contents of registers 6 and 7 and place the results in registers 6 and 7.



BRCS N, TOP	If the result is negative, disregard this pulse by going to the beginning to get the next pulse
BRCS NZ, SPR	If the upper half of the double precision difference is not zero, branch to the SPR calculation routine.
LDUB R, 13, 6	Load the upper byte of register 6 into register 13.
CMP IS, 13, 16	Compare the contents of register 13 with the magnitude 16. If the contents of register 13 is greater than 16, the time interval between pulses is greater than 52.4 milliseconds.
BRCS P, SPR	If the time interval is greater than 52.6 milliseconds, go calculate SPR.

10. UPDATE PRI, PW AND TIME. PRI and PW are updated by determining the relative size of the new value and the old. If the new value is greater than the old, 1 is added to the old and vice versa. If there is no difference, no change is made. The time is simply loaded into registers 11 and 12. On completion of this step, the four updated pulse train file words are contained in registers 9 through 12.

SUB R, 6, 10	Subtract the contents of register 10 from the contents of register 6 and place the result in register 6.
--------------	--



BRCS P,INCR	If the difference is greater than zero, the new time difference is larger. Branch to the INCRease routine which will add one to the old PRI.
BRCS N,DECR	If the difference is less than zero, the new time difference is smaller. Branch to the DECRease routine which will subtract one from the old PRI.
STORE LDR R,11,2	Load the new time located in register 2 into register 11
LDR R,12,3	Load the upper half of the new time located in register 3 into register 12.
SUB R,4,9	Subtract the contents of register 9 from the contents of register 4 and place the results in register 4. This subtracts the old pulse width from the new pulse width
BRCS P,INCP	If the result is positive, the new pulse width is greater. Branch to the increase pulse width routine (INCP) which will add 1 to the old pulse width.
BRCS N,DECP	If the result is negative, the new pulse width is smaller. Branch to the decrease pulse width routine (DECP) which will subtract 1 from the old pulse width.





11. STORE UPDATED DATA. The four updated file words are placed in memory using a stack instruction. After the stack operation, the program branches unconditionally to the beginning to get the next pulse.

STACK STK DR,8,4      Store the next four registers (9-12) into memory locations beginning with the address contained in register 8. Add 4 to the contents of register 8 on completion.

BRCS U,TOP            Unconditionally branch to the beginning (TOP) to get the next pulse.

12. START FILE. The start file routine (STAR1) is entered when the frequency file word is zero indicating that no pulse train file exists for the frequency detected. It is also entered after linking information has been prepared when the first file was not the correct one. The routine searches for the next empty pulse train file and then enters linking information into the frequency and contact files. The data is then loaded into the first entry location with -16 stored in the PRI word indicating one pulse for this file has been received. The location NEXTF is used to point to the last file activated so that the files are activated in sequence. A mask is used so that the values in NEXTF will always be modulus 64. Files are cleared by the main classification computer.

STAR1 LDR I,13,-193    Load modulo 64 mask into register 13



LDR D,6,NEXTF	Load the contents of location NEXTF into register 6
ANOT ADD IS,6,2	Register 6 contains the last file used. Add 2 to get the address of the next file entry.
AND R,6,13	Form the logical product of the contents of registers 6 and 13 and place the results in register 6. The contents of register 6 are now modulo 64.
LDR DX,8,TFILE,6	Load in register 8 the contents of the location whose address is the sum of TFILE and register 6. This is the address of the frequency associated with the next pulse train file.
BRCS NZ,ANOT	If the frequency value is not zero, branch to location ANOT which is the instruction to increment NEXTF.
STR D,6,NEXTF	Store the contents of register 6 in location NEXTF. This stores the pointer value for the pulse train file which is now being activated.
STR DX,5,TFILE,6	Store the contents of register 5 in the location whose address is the sum of TFILE and register 6. This specifies the frequency of the pulse train file and also indicates that the file is busy.



ADD IS,6,1        Add one to the contents of register 6.  
 LDR DX,8,TFILE,6    Load register 8 with the contents of  
                   the location whose address is the sum  
                   of TFILE and register 6. This is  
                   the second word of the contact file  
                   entry and is the actual address of the  
                   first word of the pulse train file.  
 STR DX,6,EFILE,7    Store the contents of register 6 in  
                   the location whose address is the sum  
                   of EFILE and register 7. This sets the  
                   link between the frequency word and  
                   the pulse train file entry address.  
 LDR R,9,4        Load register 9 with the contents of  
                   register 4 (pulse width).  
 LDR IS,10,-16      Load register 10 with the number -16  
                   (pulse counter)  
 LDR R,11,2        Load register 11 with the contents of  
                   register 2 (time, lower half)  
 LDR R,12,3        Load register 12 with the contents of  
                   register 3 (time upper half). The  
                   pulse data is contained in registers  
                   9 through 12.  
 STK DR,8,4        Store the contents of registers 9  
                   through 12 in memory locations beginning  
                   with the address contained in register 8.  
 BRCS U,TOP        Branch unconditionally to the beginning  
                   (TOP) to get the next pulse.



13. WRONG FILE. The routine NTRY is entered when the pulse width of the previous pulse train file was not within limits. This routine establishes linking to the next pulse train file by taking the upper half of the frequency file word and placing it into register 7 and branching to FLINK if a file exists or branching to routine STAR2 if another file has not been started. FLINK is the execution step that enters the frequency file. The contents of register 7 will now be the overflow location in the file. STAR2 establishes the initial linking for establishing multiple files for the same frequency.

NTRY LDUB R,14,6	Load register 14 with the upper byte of the contents of register 6.
BRCS Z,STAR2	If the upper byte of register 6 was zero, another pulse train file has not been established for this frequency. Branch to STAR 2 and establish one.
LDR R,7,14	Load register 7 with the contents of register 14.
BRCS U.FLINK	Unconditionally branch to FLINK. FLINK is the location of the FIND CONTACT FILE NR sequence.

14. START FILE (2) The routine STAR2 is entered when two or more files are established for one frequency. On entry, the lower byte of register 6 always contains the relative address of the last frequency file accessed and the upper byte is always zero indicating that there are no





more files in the chain. STAR2 sets the upper half of this entry word equal to the address of the next entry for this frequency and stores it in the word's proper location.

STAR2 then branches to routine STAR1 which finds the next empty pulse train file.

LDR D,14,OFLOW      Load register 14 with the contents of location OFLOW. OFLOW contains the relative address of the next available frequency file overflow location.

XCHB R,13,14        Load register 13 with the contents of register 14 with the bytes exchanged. This places the overflow location relative address in the upper byte of register 14.

ADD R,6,13          Add the contents of register 13 to the contents of register 6 and place the results in register 6. This assembles a word in register 6 which consists of two separate bytes. The lower byte is the relative address of the frequency file entry that lead to the incorrect pulse train file. The upper byte is the relative address of the frequency file entry which will lead to the correct pulse train file for the pulse width of the current pulse.



STR DX,6,EFILE,7	Store the contents of register 6 in the location whose address is the sum of EFILE and register 7.
LDR R,7,14	Put proper relative address into register 7
ADD IS,14,1	Add one to the contents of register 14
STR D,14,OFLOW	Store the contents of register 14 in location OFLOW. The contents of OFLOW now point to the next available over- flow location.
BRCS U,STAR1	Unconditionally branch to STAR1 where the next pulse train file will be activated.

15. ENOUGH PULSES TO CALCULATE PRI? Routine BUILD is entered when it has been determined that the PRI word of a pulse train file is less than zero indicating the file is still building. The number one is added to the negative pulse counter and it is tested. If the counter is now zero, the current pulse is the last one needed to calculate the PRI and the program branches to the calculate PRI routine (PRI). If the counter is still negative, the program then continues to add the pulse data to the pulse train file.

ADD IS,10,1	Add 1 to the contents of register 10.
BRCS Z,PRI	If the counter is now zero, branch to the calculate PRI routine (PRI).

16. ADD INFORMATION TO THE DATA SET. The pulse counter is stored. The proper location of the current pulse data



is determined by adding 16 to the pulse counter value. The result is the number of the pulse in the current pulse train. This number is then multiplied by 4 (shifted left 2 bits) to determine the address of the first data word relative to the start of the file. The data is then stored after checking to ensure it is valid data.

STR RX,10,8,1      Store the contents of register 10 in the location whose address is the sum of registers 8 and 1. Register 8 contains the address of the first location of the pulse train file. Register 1 contains the number 1. The pulse counter is stored in the second word of the file.

ADD IS,10,16      Add 16 to the contents of register 10. The result is the number of the slot for the current pulse data.

SHS LL,10,2      Shift the contents of register 10 left two bits. This multiplies the contents of register 10 by 4.

ADD R,8,10      Add the contents of register 10 to the contents of register 8 and place the results in register 8. This forms the actual address of the first word of the locations for the current pulse.

LDR R,5,8      Load register 5 with the contents of register 8.



ADD IS,5,-2	Subtract 2 from the contents of register 5. This forms the address of the time of arrival of the previous pulse of the current pulse train.
LDRM DR,5,2	Load registers 6 and 7 with the contents of two adjacent locations whose addresses start at the contents of register 5.
LDR R,11,2	Load register 11 with the contents of register 2.
LDR R,12,3	Load register 12 with the contents of register 3. The time of arrival of the current pulse has been copied into registers 11 and 12.
DSUB R,2,6	Double precision subtract the contents of registers 6 and 7 from the contents of registers 2 and 3 and place the results in registers 2 and 3. This puts the time interval between pulses in registers 2 and 3.
BRCS N,TOP	If the time difference is negative, branch to the beginning disregarding the current pulse.
BRCS Z,GOOD	If the upper half of the time difference is zero, the time is considered a PRI and the next instruction is not executed.





LDR	IS,2,0	Load register 2 with the number 0. This will cause zero to be stored for the interval between pulses.
GOOD	LDR R,10,2	Load the single precision value of the interval between pulses into register 10 from register 2.
LDR	R,9,4	Load register 9 with the contents of register 4 (pulse width). The contents of registers 9-12 is now the data associated with the current pulse.
STK	DR,8,4	Store the contents of registers 9-12 in locations whose addresses start with the contents of register 8. Add 4 to the contents of register 8.
BRCS	U,TOP	Unconditionally branch to the beginning (TOP) to get the next pulse.

17. CALCULATE AVERAGE PRI AND PW. When the seventeenth pulse of a pulse train file is received the program enters PRI which calculates the average PRI and pulse width of the pulse train file. The time interval between the last two pulses is calculated and then all sixteen intervals and the last sixteen pulse widths are added. The program then branches to PEND where the sums are divided by 16 to form the average.

PRI	LDR	IS,1,-15	Load register 1 with the number 15. This is used as a counter
-----	-----	----------	--



ADD IS,8,64	Add 64 to the contents of register 8. Register 8 now contains the required address for the RETURN instruction to return the last pulse train file data set.
RET DR,8,4	Load registers 9-12 with the last data set.
LDR R,6,2	Load register 6 with the contents of register 2.
LDR R,7,3	Load register 7 with the contents of register 3. The time of arrival of the current pulse is copied into registers 6 and 7.
DSUB R,6,11	Double precision subtract the contents of registers 11 and 12 from the contents of registers 6 and 7. The last time interval is contained in registers 6 and 7.
BRCS N,TOP	If the time difference is negative, disregard this pulse.
LDR IS,11,0	Load 0 into register 11.
LDR R,12,6	Set PRI standard.
LP2 ADD R,4,9	Add the contents of register 9 to the contents of register 4 and place the sum in register 4. This accumulates the sum of the pulse widths.



DADD R,6,10	Double precision add the contents of registers 10 and 11 to the contents of registers 6 and 7.
ADD IS, 1,1	Add 1 to the contents of register 1. This steps the counter.
BRCS Z,PEND	If the counter is zero, all pulse data has been summed. Branch to the divide routine (PEND).
ADD IS,8,-2	Set address for the next data set.
RET DR,8,2	Return the pulse width and the time interval from the previous data set.
SUB R,10,12	Find the difference between this time interval and the PRI standard.
BRCS P,LP3	If the difference is positive, test the results at LP3.
CMP IS,10,-4	Compare the difference, when negative, with the magnitude -4.
BRCS N,NG	If the difference is less than -4, go throw the pulse out.
ADD R,10,12	Restore the time interval value in register 10.
BRCS U,LP2	Unconditionally branch to LP2 to sum the data.
LP3 CMP IS,10,4	If the difference between the time interval and the PRI standard is positive, compare the difference to the magnitude 4.



BRCS	P,NG	If the difference is greater than 4, go throw the pulse out.
ADD	R,10,12	Restore the time interval value in register 10.
BRCS	U,LP2	Unconditionally branch to LP2 to sum the data.
NG LDR	R,10,12	Replace the time interval with the value of the PRI standard.
BRCS	U,LP2	Unconditionally branch to LP2 and sum the data.
PEND SHD	RA,6,4	Double precision shift right regis- ters 6 and 7 4 bits (divide by 16).
SHS	RA,4,4	Shift register 4 right 4 bits to divide by 16.
RET	DR,8,2	Return the first time of arrival in the file.
ADD	IS,8,2	Set the address for the second data block.
LDR	IS,11,0	Load 0 into register 11.
LDR	IS,12,0	Load 0 into register 12.
STK,DR	8,4	Store the contents of registers 9-12 in locations whose addresses start with the contents of register 8. This stores the times required to calculate SPR and sets the initial value of SPR to 0.





LDR	R,9,4	Load register 9 with the contents of register 4.
LDR	R,10,6	Load register 10 with the contents of register 6.
LDR	R,11,2	Load register 11 with the contents of register 2.
LDR	R,12,3	Load register 12 with the contents of register 3. The entire data set is loaded into registers 9-12.
ADD	IS,8,-8	Set the address of the first data block of this pulse train.
STK	DR,8,4	Store the contents of registers 9-12 in locations whose addresses start with the contents of register 8. Add 4 to the contents of register 8.
BRCL	U,TOP	Branch to the beginning to get the next pulse.

18. CALCULATE SPR AND UPDATE TIME. Routine SPR is entered when a large time difference is noted between the current pulse and the previous pulse of a closed pulse train file. The time that the last sequential group of pulses arrived is accessed and subtracted from the current time to determine the antenna scan time. The current time and the SPR are stored in the file.

SPR ADD IS,1,1      Increment address pointer.

LDR RX,11,8,1      Load register 11 with the contents of the location whose address is the sum



of register 8 and register 1. This is the start of the time that the last antenna scan was received.

ADD IS,1,1	Load second half of this time word
LDR RX,12,8,1	into register 12.
LDR R,6,2	Move the new time of arrival into
LDR R,7,3	working registers.
DSUB R,6,11	Double precision subtract the contents
	of registers 11 and 12 from the contents
	of registers 6 and 7. This is the SPR
	value.
LDR IS,1,4	Set the address pointer
STR RX,2,1,8	Store the new time of arrival
ADD IS,1,1	
STR RX,3,1,8	
ADD IS,1,1	
STR RX,6,1,8	Store the value of the SPR
ADD IS,1,1	
STR RX,7,1,8	
BRCS U,STORE	Unconditionally branch to STORE and
	finish updating the pulse information.



## APPENDIX E

### DATA SIMULATION PROGRAM GLOSSARY OF VARIABLES AND FORTRAN LISTING

#### DATA SIMULATION PROGRAM GLOSSARY OF VARIABLES

ANG(I,J)	True pointing angle of the antenna on the Jth emitter on the Ith platform
ANT(I,J0	Antenna scan rate of the Jth emitter on the Ith platform
BIN	IFM frequency bin size
BEAM	Input value of antenna beam width
BNG(I)	True bearing of the Ith platform
BNGI	Computation value of BNG(I)
BW(I,J)	Antenna beam attenuation factor of the Jth emitter on the Ith platform
CON1	Conversion factor used in converting from antenna beam width in degrees to the antenna attenuation factor
CON2	Conversion factor used in converting from transmitter peak power to transmitter total effective radiated power
CSEI	Input value of the course of the Ith platform
CSEO	Input value of the course of the IFM
D1	Distance to CPA
D2	Distance to the maximum range at which an emitter can be detected



DEGR	Conversion factor to convert angles in degrees to angles in radians
DEL	Time after the start of the simulation that an emitters first pulse is transmitted or that an emitter is within its maximum detection range
F(I,J)	Transmitted frequency of the Jth emitter on the Ith platform
FMAX	Maximum receive frequency of the IFM
FMIN	Minimum receive frequency of the IFM
FREQ	Input value of the operating frequency of an emitter
FSCALE	Conversion factor for converting from Mega units to units
GAIN	Input value of antenna gain
ICT	Counter for number of pulses received by the IFM
IF(I,J)	Selector for the desired type of frequency variation
INEXT(L)	Platform subscript of the second or more pulses when more than one pulse is received simultaneously by the IFM
IPRI(I,J)	Selector for the desired type of PRI variation
IPT(I,J)	Selector for the desired type of output power variation





IPW(I,J)	Selector for the desired type of pulse width variation
ISCAN(I,J)	Selector for the desired type of scan rate variation
ITEMP	Platform subscript of the current pulse received by the IFM
JNEXT(L)	Emitter subscript used for multiply received pulses
JTEMP	Emitter subscript of the current pulse received by the IFM
N	Bin number of the frequency of the received pulse
NBIN	Number of frequency bins in the bandwidth of the IFM
NGAUS	Integer calling argument for the Gaussian Distribution Random Number Generator
NMTR(I)	Number of emitters on the Ith platform
NOUT(K)	Array used to prepare output data for the ATAC Simulator
NPW	Integer representation of pulse width as required by the ATAC Simulator
NTIME	Integer representation of simulation time
NTIME1	Lower half of the double precision time value required by the ATAC Simulator
NTIME2	Upper half of the double precision time value required by the ATAC Simulator



NUNI	Integer calling argument for the Uniform Distribution Random Number Generator
PI	3.1415926
PI2	$PI/2$
POWER(I,J)	Total effective transmitted power of the Jth emitter on the Ith platform
POWIJ	Calculation value of POWER(I,J)
PRI(I,J)	PRI of the Jth emitter on the Ith platform
PRIN	Input value of PRI
PSCALE	Conversion factor for converting from milli units to units
PTRANS	Input value of transmitter power
PULSE	Calculation value of PW(I,J)
PW(I,J)	Pulse width of the Jth emitter on the Ith platform
R	Range of the Ith platform
RCVBNG	Bearing from which the current pulse arrived
RCVR	Frequency of the received pulse
RECSIG	Signal level of the received pulse
RCSE	Direction of Relative Motion
RDEG	Conversion factor for converting angles in radians to angles in degrees
RMAX	Maximum range at which an emitter can be detected
SCAN	Subroutine that calculates an antenna true pointing angle and its gain in the direction of the IFM



SCNMIN	The minimum value of antenna gain for which an emitter can be detected by the IFM
SEND(I,J)	Time of transmission of a pulse from the Jth emitter on the Ith platform
SIGFRQ(I,J)	Frequency of the transmitted pulse
SPDI	Input speed of the Ith platform
SPDO	Input speed of the IFM
TF	Simulation stop time
THETAI	Bearing of the CPA of the Ith platform
THRESH	Threshold sensitivity of the IFM
TINT	Minimum time measurement capability of the system utilizing the IFM
TNEXT(I,J)	Time of arrival at the IFM of the next pulse transmitted by the Jth emitter on the Ith platform .
TO	Simulation start time
TOF	Time required for the propagation of a pulse from an emitter to the IFM
TSCALE	Conversion factor for converting from Kilo units to units
TSKTS	Conversion factor for converting from knots to yards per second
TT	Calculation value of TNEXT(I,J)
TWOPI	$2\pi$
UPDATE	Subroutine that calculates the time of arrival of the next pulse from an emitter
VL	Velocity of Light



VTI	Total relative velocity of the Ith platform
VX(I)	Relative velocity of the Ith platform in the X direction
VXI	Calculation value of VX(I)
VXO	Velocity of the IFM in the X direction
VY(I)	Relative velocity of the Ith platform in the Y direction
VYI	Calculation value of VY(I)
VYO	Velocity of the IFM in the Y direction
WSCALE	Conversion factor for converting from micro units to units
X(I)	Relative X position of the Ith platform
XI	Input X position of the Ith platform
XO	Input X position of the IFM
Y(I)	Relative Y position of the Ith platform
YDS	Conversion factor for converting knots to yards per second
YI	Input Y position of the Ith platform
YO	Input Y position of the IFM
Z(I)	Relative Z position of the Ith platform
ZI	Input Z position of the Ith platform
ZO	Input Z position of the IFM





DATA SIMULATION PROGRAM DATA DECK SETUP

1. The data deck for use of the DSP is segregated into four basic parts.

- a. (Three cards) IFM Platform Information
- b. (One card) Emitter Platform Information
- c. (Two cards) Emitter Information
  - 
  - 
  - 
  - (Up to five emitters)
  -
- b. (One card) Emitter Platform Information
- c. (Two cards) Emitter Information
  - 
  - 
  - (Up to ten platforms)
- d. (One card) End of data card with any negative number in columns 21-30

2. The format for each required card is shown below.

- a. IFM Platform Information

Card	Columns	Format	Variable	Units
1	1-10	I10	NUNI	Odd Integer Right Justified
	11-20	I10	NGAUS	Odd Integer Right Justified
	21-30	F10.0	VL	10 <sup>6</sup> YDS/SEC
	31-40	F10.0	TO	Seconds
	41-50	F10.0	TF	Seconds
	51-60	F10.0	TINT	Microseconds
	61-70	F10.0	THRESH	dbm



2	1-10	F10.0	XO	Nautical miles
	11-20	F10.0	YO	Nautical miles
	21-30	F10.0	ZO	Feet
	31-40	F10.0	CSEO	Degrees clockwise from North
	41-50	F10.0	SPDO	Knots
	51-60	F10.0	FMAX	MHZ
	61-70	F10.0	FMIN	MHZ
3	1-10	I10	NBIN	Integer
				Right Justified

b. Emitter Platform Information

Card	Columns	Format	Variable	Units
1	1-10	F10.0	XI	Nautical miles
	11-20	F10.0	YI	Nautical miles
	21-30	F10.0	ZI	Feet
	31-40	F10.0	CSEI	Degrees clockwise from North
	41-50	F10.0	SPDI	Knots
	51-51	I1	NMTR(I)	Integer

c. Emitter Information

Card	Columns	Format	Variable	Units
1	1-10	F10.0	FREQ	MHZ
	11-20	F10.0	PRI	milliseconds
	21-30	F10.0	PW	microseconds
	31-40	F10.0	PTRANS	Kilowatts
	41-50	F.0.0	BEAM	Degrees



	51-60	F10.0	GAIN	db
	61-70	F10.0	SCAN	Seconds per revolution
2	1	I1	IF(I)	Integer
	2	I1	IPRI(I)	Integer
	3	I1	IPW(I)	Integer
	4	I1	IPT(I)	Integer
	5	I1	ISCAN(I)	Integer

d. End of data card

Columns 21-30

Any negative number

3. The program listed herein does not include coding for use of the parameter variations. This feature can easily be added by using utility subroutines GAUS and RANDU or any other random number generation scheme.

4. The program listed herein contains coding for only two types of antenna scan--circular and steady. Coding for additional types was being prepared when it was determined what the run times for the ATAC Simulations were going to be. As the simulations take very long periods to run on modest data sets, the addition of the additional features was delayed. Coding to add additional scan types can be readily accomplished.

5. The units of the input variables were selected so that values could be coded without the need for using the exponential format. It is felt that this feature will help reduce data deck format errors by allowing the input data



to be placed anywhere within the 10 column field as long as a decimal place is used somewhere.





```

0000 DSP
0010 DSP
0020 DSP
0030 DSP
0040 DSP
0050 DSP
0060 DSP
0070 DSP
0080 DSP
0090 DSP
0100 DSP
0110 DSP
0120 DSP
0130 DSP
0140 DSP
0150 DSP
0160 DSP
0170 DSP
0180 DSP
0190 DSP
0200 DSP
0210 DSP
0220 DSP
0230 DSP
0240 DSP
0250 DSP
0260 DSP
0270 DSP
0280 DSP
0290 DSP
0300 DSP
0310 DSP
0320 DSP
0330 DSP
0340 DSP
0350 DSP
0360 DSP
0370 DSP
0380 DSP
0390 DSP
0400 DSP
0410 DSP
0420 DSP
0430 DSP
0440 DSP
0450 DSP
0460 DSP
0470 DSP

DATA SIMULATION PROGRAM (DSP)

THE DSP GENERATES SIMULATION DATA FOR TESTING IFM DIGITAL
PROCESSOR ALGORITHMS. FOR DETAILED EXPLANATION OF THE PROGRAM
AND INSTRUCTION FOR ITS USE, SEE NPS THESIS:

ELECTRONIC WARFARE APPLICATIONS OF
SPECIAL PURPOSE MICROPROGRAMMABLE MINICOMPUTERS
LCDR P. D. FRAZER, JUNE 1974

COMMON X(10),Y(10),Z(10),VX(10),VY(10),VZ(10),TINT,VXO,VYO,VZO,
10,THRESH,PI,PI2,SCNMIN,PRIN,SIGFRQ(10,5),PRI(10,5),PW(10,5),PANG(10,5),
20,5),BW(10,5),SEND(10,5),TNEXT(10,5),SIGNAL(10,5),ANT(10,5),FMAX,FMIN,BIN,
30,5),XO,YO,ZO,CSEO,SPDO,VL,TWOPI,RDEGR,TO,TF,FMEX,FMIN,BIN,
4IF(10,5),I,PI(10,5),IPW(10,5),IPT(10,5),ISCAN(10,5),INEXT(10,5),JNEX
5T(10),NUNI,NGAUS,NMTR(10),NCUT(8)

INITIALIZE CONSTANTS

PI2=AR SIN(1.0)
PI=2.*PI2
TWOPI=4.*PI2
RDEGR=180./PI
DEGR=PI/180.
CCCN1=PI*58.9
CCCN2=10.*ALOG10(4.*PI)
TSKTS=2025.4
YCS=2025.4
FSCALE=1.E6
PSCALE=1.E3
WSCALE=1.E-5
IIC=0

SET IFM INFORMATION

READ (5,18) NUNI,NGAUS,VL,TO,TF,TINT,THRESH
VL=VL*FSCALE
TINT=TINT*WSCALE

```



DSP 0480  
 DSP 0490  
 DSP 0500  
 DSP 0510  
 DSP 0520  
 DSP 0530  
 DSP 0540  
 DSP 0550  
 DSP 0560  
 DSP 0570  
 DSP 0580  
 DSP 0590  
 DSP 0600  
 DSP 0610  
 DSP 0620  
 DSP 0630  
 DSP 0640  
 DSP 0650  
 DSP 0660  
 DSP 0670  
 DSP 0680  
 DSP 0690  
 DSP 0700  
 DSP 0710  
 DSP 0720  
 DSP 0730  
 DSP 0740  
 DSP 0750  
 DSP 0760  
 DSP 0770  
 DSP 0780  
 DSP 0790  
 DSP 0800  
 DSP 0810  
 DSP 0820  
 DSP 0830  
 DSP 0840  
 DSP 0850  
 DSP 0860  
 DSP 0870  
 DSP 0880  
 DSP 0890  
 DSP 0900  
 DSP 0910  
 DSP 0920  
 DSP 0930  
 DSP 0940  
 DSP 0950

```

READ (5,19) XO,YO,ZO,CSEO,SPDO,FMAX,FMIN
READ (5,22) NBIN
FMAX=FMAX*FSCALE
FMIN=FMIN*FSCALE
BIN=(FMAX-FMIN)/FLOAT(NBIN)
WRITE (6,25) XO,YO,ZO,CSEO,SPDO,FMAX,BIN,NBIN
WRITE (6,26) THRESH
CSEO=CSEO*DEGR
SPDO=SPDO*TSKTS
XC=XO*YDS
YC=YO*YDS
ZC=ZO/3.
VXC=SPDO*SIN(CSEO)
VYC=SPDO*COS(CSEO)
I=1

```

CCCC

GET EMITTER PLATFORM INFORMATION

```

1 READ (5,20) XI,YI,ZI,CSEI,SPDI,NMTR(I)
IF (ZI.LT.0.) GO TO 11
WRITE (6,27) I,XI,YI,ZI,CSEI,SPDI
CSEI=CSEI*DEGR
SPDI=SPDI*TSKTS
VXI=SPDI*SIN(CSEI)-VXO
VYI=SPDI*COS(CSEI)-VYO
XI=XI*YDS-XO
YI=YI*YDS-YO
ZI=ZI/3.
VXI=SQRT(VXI**2+VYI**2)
VYI=SQRT(VXI**2+VYI**2)
RCSEI=ATAN2(VXI,VYI)
BNGI=ATAN2(XI,YI)
TCF=R/VL
X(I)=XI
Y(I)=YI
VY(I)=VYI
VY(I)=VYI
BNGI(I)=BNGI
THETA(I)=ABS(PI-BNGI+RCSEI)
IF (THETA(I).GE.PI2) GO TO 2
IF (THETA(I).GE.PI)
  DI=R*COS(THETA)
  CPA=R*SIN(THETA)
  GO TO 3
CPA=R
3 JJ=NMTR(I)

```



GET EMITTER INFORMATION

[illegible]

### CALCULATE THE TOA OF THE FIRST PULSE

[illegible]









CC

```

16  RCVSIG=SIGNA(I TEMP,JTEMP)
    RCVR=SIGRQ(I TEMP,JTEMP)
    N=(RCVR-FMIN)/BIN+1.
    RCVBNG=BNG(I TEMP)*RDEG
    IF (RCVBNG.LT.0.0) RCVBNG=RCVBNG+360.
    ICT=ICT+1
    NPW=1.0E7*PW(I TEMP,JTEMP)
    TNEXT=TNEXT+1.0E7/256.
    NTIME1=MOD(NTIME,65536)
    NTIME2=NTIME/65536
    NRITE(IJ+1)=N
    NOUT(IJ+2)=NTIME1
    NOUT(IJ+3)=NTIME2
    NOUT(IJ+4)=NPW
    IFJ=1
    IF (IJ.LT.8) GO TO 17
    IFJ=0
    NRITE(7,24) NOUT
    IF (ICT.GE.1024) STOP
17  GO CALCULATE THE TGA OF THE NEXT PULSE FROM THIS EMITTER

    CALL UPDATE (I TEMP,JTEMP)
    IF (L.EQ.0) GO TO 12
    ITEMP=JNEXT(L)
    JTEMP=JNEXT(L)
    L=L-1
    GO TO 16

18  FFORMAT (2,110,6E10.0)
19  FFORMAT (8E10.0)
20  FFORMAT (5E10.0,11)
21  FFORMAT (1011)
22  FFORMAT (110)
23  FFORMAT (140,5110,1PE20.4)
24  FFORMAT (8,116,1X)
25  FFORMAT (1,10,UNIT INFORMATION,/,,'OINITIAL POSITION:',T40,
    1  T120,,'NR BINS',,SPEED:',T70,'FREQUENCY COVERAGE',T100,'BINSIZE',
    2  T120,,'HOLD =',F8.1,,'O3M:')
26  FFORMAT (1,120,,'F16.1, F14.1,1PE20.4, '-',E12.4,E15.4,T120,17)
27  FFORMAT (1,120,,'TRESH INFORMATION',/,,'OPLATFORM',T15,'INITIAL POSITION',DSP

```

CCCC

C



```

1 T50,'COURSE',T60,'SPEED',/,I5,T15,3F10.1,T50,F6.0,T60,F5.0,/,POWER,
2 I0,T10,'EMIN',T83,T23,'AM WIDTH',T36,T39,PRI,T49,'PW',T62,'TRANS POWER',
3 T75,'ANT GAIN',T20,T14,'CIRADY',F5,2,' SPR')
28 FORMAT('+',T14,T114,'OUT OF RANGE')
29 FORMAT('+',T14,T114,'DATA',/,',',0,T48,'PULSE',2X,'FREQ BIN',2X,
30 FORMAT('EMITTER TIME',4X,'PW',10X,'TOA',)
31 FORMAT('PRECISION',1,T48,'TIME',4X,'PW',10X,'TOA',)
32 C
END

```

```

DSP 2400
DSP 2410
DSP 2420
DSP 2430
DSP 2440
DSP 2450
DSP 2460
DSP 2470
DSP 2480
DSP 2490

```













OUTPUT DATA

PULSE NR	FREQ BIN	DBLE WORD TIME	PW	TIME
1	23	0	42	-4.000000E-06
2	39	0	19	-1.000000E-06
3	64	0	14	-1.245000E-03
4	23	487	49	1.249000E-03
5	23	517	49	2.249000E-03
6	23	1146	49	3.745000E-03
7	23	1195	49	4.745000E-03
8	23	2243	49	5.998000E-03
9	23	2243	49	6.244000E-03
10	23	2294	49	7.494000E-03
11	23	3333	49	8.744000E-03
12	23	3333	49	9.994000E-03
13	43	3333	35	1.099000E-02
14	39	4239	53	1.099000E-02
15	26	4463	41	1.129470E-02
16	40	4467	49	1.129980E-02
17	40	4482	49	1.129980E-02
18	29	4483	40	1.123450E-02
19	23	4451	50	1.123190E-02
20	29	5555	50	1.133740E-02
21	29	5555	49	1.133740E-02
22	29	5555	49	1.142980E-02
23	40	5555	49	1.142980E-02
24	23	5555	49	1.149970E-02
25	29	5555	30	1.151330E-02
26	29	5555	40	1.151450E-02
27	29	6667	44	1.162450E-02
28	29	6667	49	1.170990E-02
29	29	7041	40	1.179970E-02
30	29	7041	40	1.180990E-02
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